SSD1316

Advance Information

128 x 39 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: IC Revision history of SSD1316 Specification

Version	Change Items	Effective Date
0.10	1st Release	15-Jul-11
1.0	Advance Information Release Modify from SSD1316 Product Preview R0.10 Update the Charge Pump 8D Command Update the DC characteristics Update the AC characteristics	10-Oct-11
1.1	Advance Information Release Modify from SSD1316 Advance Information R1.0 Revise typo for ADh command for internal IREF selection Update V_{BAT} and the Charge Pump 8Dh command Update the DC characteristics Revise Figure 9.10 and Figure 9.11 for continuous scrolling Add Content Scrolling Setup details	16-Apr-12
1.2	Advance Information Release Modify from SSD1316 Advance Information R1.1 Update Contrast Control 81h command Update Typical Frequency in AC characteristics	08-Nov-13

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TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1316 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 39 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1316 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8080 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and Bluetooth headset and Medical devices, etc.

2 FEATURES

- Resolution: 128 x39 dot matrix panel
- Power supply
  - V_{DD} = 1.65V ~ 3.3V, < V_{BAT} for IC logic
  - V_{BAT} = 3.0V ~ 4.2V for charge pump regulator circuit
  - V_{CC} = 7V~15V for Panel driving
- For matrix display
- OLED driving output voltage, 15V maximum
- Segment maximum source current: 160uA
- Common maximum sink current: 20mA
- 256 step contrast brightness current control
- Embedded 128 x 39 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 /4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Internal charge pump regulator
- Internal regulated V_{COMH} or external V_{COMH}
- Internal I_{REF} or external I_{REF}
- Programmable Frame Rate
- Programmable Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG , COF
- Wide range of operating temperature: -40°C to 85°C

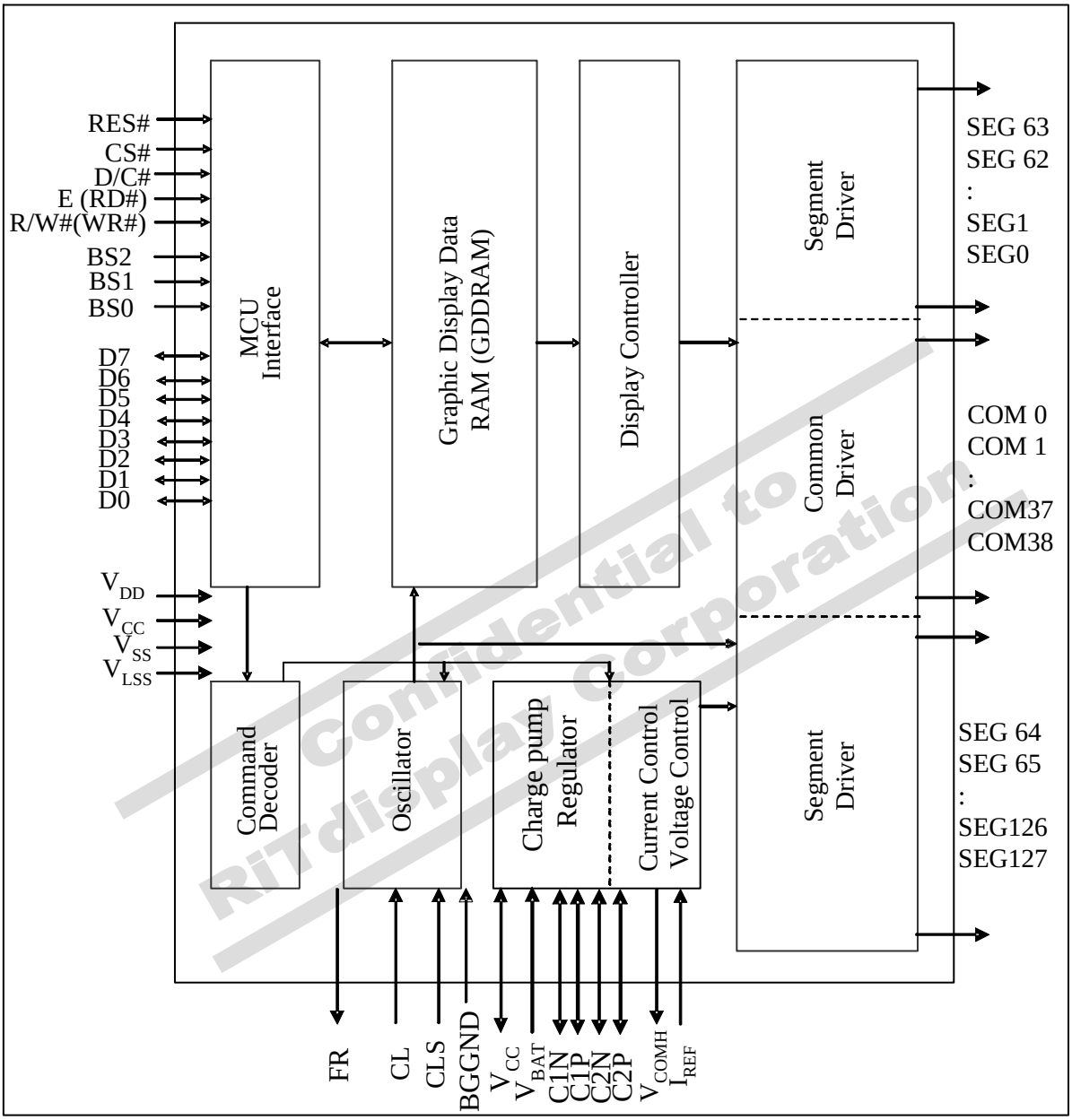
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD1316Z	128	39	COG	-

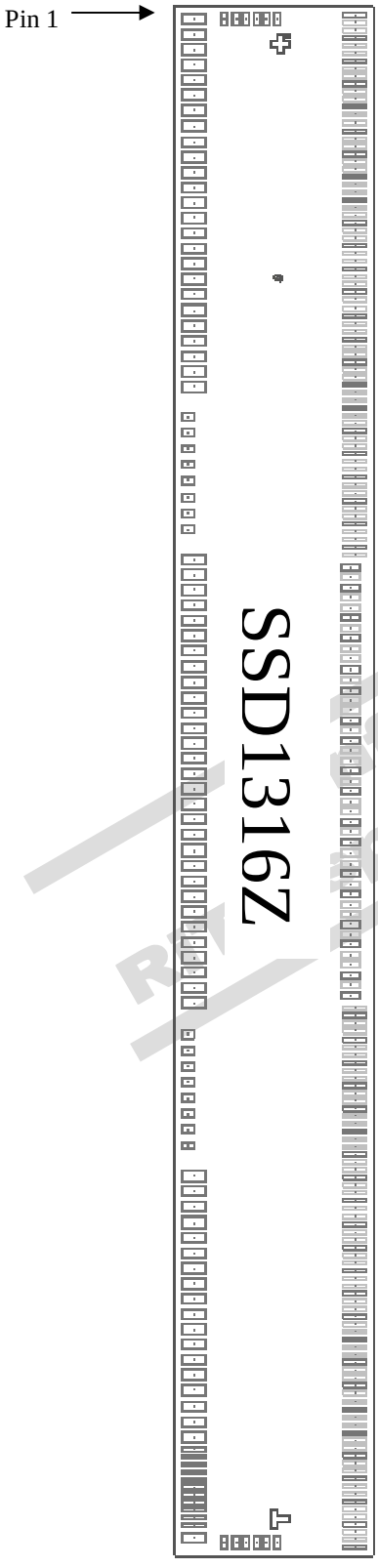
4 BLOCK DIAGRAM

Figure 4-1 : SSD1316 Block Diagram



5 DIE PAD FLOOR PLAN

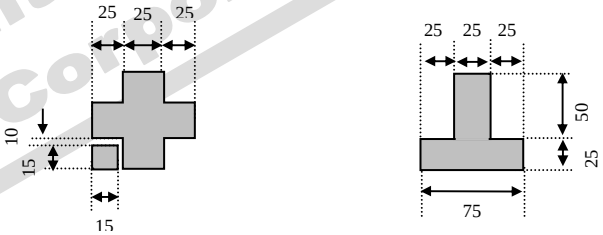
Figure 5-1 : SSD1316Z Die Drawing



Die Size (after sawing)	6.08mm +/- 0.05mm x 0.79mm +/- 0.05mm
Die Thickness	300 um ± 15 um
Min I/O pad pitch	60 um
Min SEG pad pitch	30.2 um
Min COM pad pitch	40 um
Bump Height	Nominal 12 um

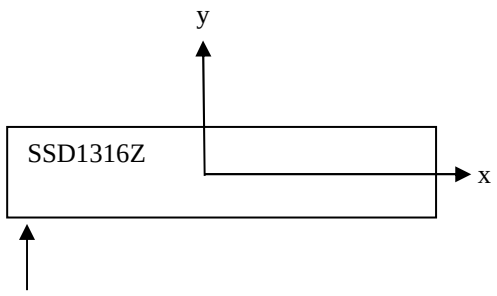
Bump Size		
Pad #	**X [um]**	**Y [um]**
1~25, 34~63, 72~89, 101	40	95
26~33, 64~71	30	50
90~100	15	95
102~107, 293~298	50	25
108~178, 222~292	15.2	94
179~221	25	77

Alignment mark	Position	Size
T shape	(2890, 19.5)	75um x 75um
+ shape	(-2890, 19.5)	75um x 75um



Note

(1) Diagram showing the Gold bumps face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold.



Pad 1, 2, 3 .... -> 101

Gold Bumps face up

Table 5-1 : SSD1316Z Bump Die Pad Coordinates

Pin number	Pin name	X	Y
1	NC	-2987.5	-315
2	C2N	-2927.5	-315
3	C2N	-2867.5	-315
4	C2N	-2807.5	-315
5	C2N	-2747.5	-315
6	C2P	-2687.5	-315
7	C2P	-2627.5	-315
8	C2P	-2567.5	-315
9	C2P	-2507.5	-315
10	C1P	-2447.5	-315
11	C1P	-2387.5	-315
12	C1P	-2327.5	-315
13	C1P	-2267.5	-315
14	C1N	-2207.5	-315
15	C1N	-2147.5	-315
16	C1N	-2087.5	-315
17	VBAT	-2027.5	-315
18	VBAT	-1967.5	-315
19	VBAT	-1907.5	-315
20	VCC	-1847.5	-315
21	VCC	-1787.5	-315
22	VCC	-1727.5	-315
23	VCOMH	-1667.5	-315
24	VCOMH	-1607.5	-315
25	VCOMH	-1547.5	-315
26	VLSS	-1427.5	-337.5
27	VLSS	-1365	-337.5
28	VLSS	-1302.5	-337.5
29	VLSS	-1240	-337.5
30	VSS	-1177.5	-337.5
31	VSS	-1115	-337.5
32	VSS	-1052.5	-337.5
33	VSS	-990	-337.5
34	VDD	-870	-315
35	VDD	-810	-315
36	FR	-750	-315
37	VSS	-690	-315
38	CS#	-630	-315
39	RES#	-570	-315
40	D/C#	-510	-315
41	VSS	-450	-315
42	R/W#(WR#)	-390	-315
43	E/RD#	-330	-315
44	D0	-270	-315
45	D1	-210	-315
46	D2	-150	-315
47	D3	-90	-315
48	VSS	-30	-315
49	D4	30	-315
50	D5	90	-315
51	D6	150	-315
52	D7	210	-315
53	CL	270	-315
54	VSS	330	-315
55	CLS	390	-315
56	VDD	450	-315
57	VDD	510	-315
58	BS0	570	-315
59	VSS	630	-315
60	BS1	690	-315
61	VDD	750	-315
62	BS2	810	-315
63	VSS	870	-315
64	BGGND	990	-337.5
65	VSS	1052.5	-337.5
66	VSS	1115	-337.5
67	VSS	1177.5	-337.5
68	VLSS	1240	-337.5
69	VLSS	1302.5	-337.5
70	VLSS	1365	-337.5
71	VLSS	1427.5	-337.5
72	VBREF	1547.5	-315
73	VSS	1607.5	-315
74	VSS	1667.5	-315
75	GPIO0	1727.5	-315
76	GPIO1	1787.5	-315
77	VDD	1847.5	-315
78	VDD	1907.5	-315
79	NC	1967.5	-315
80	IREF	2027.5	-315
81	VCOMH	2087.5	-315
82	VCOMH	2147.5	-315
83	VCOMH	2207.5	-315
84	VCOMH	2267.5	-315
85	VCC	2327.5	-315
86	VCC	2387.5	-315
87	VCC	2447.5	-315
88	VCC	2507.5	-315
89	NC	2567.5	-315
90	TR0	2616	-315
91	TR1	2646	-315
92	TR2	2676	-315
93	TR3	2706	-315
94	TR4	2736	-315
95	VSS	2766	-315
96	TR5	2796	-315
97	TR6	2826	-315
98	TR7	2856	-315
99	TR8	2886	-315
100	TR9	2916	-315
101	NC	2964.5	-315
102	NC	2986.4	-193.425
103	NC	2986.4	-153.425
104	NC	2986.4	-113.425
105	NC	2986.4	-73.425
106	NC	2986.4	-33.425
107	NC	2986.4	6.575
108	VCC	3003.4	316.5
109	VCC	2973.2	316.5
110	VCC	2943	316.5
111	SEG63	2912.8	316.5
112	SEG62	2882.6	316.5
113	SEG61	2852.4	316.5
114	SEG60	2822.2	316.5
115	SEG59	2792	316.5
116	SEG58	2761.8	316.5
117	SEG57	2731.6	316.5
118	SEG56	2701.4	316.5
119	SEG55	2671.2	316.5
120	SEG54	2641	316.5
121	SEG53	2610.8	316.5
122	SEG52	2580.6	316.5
123	SEG51	2550.4	316.5
124	SEG50	2520.2	316.5
125	SEG49	2490	316.5
126	SEG48	2459.8	316.5
127	SEG47	2429.6	316.5
128	SEG46	2399.4	316.5
129	SEG45	2369.2	316.5
130	SEG44	2339	316.5
131	SEG43	2308.8	316.5
132	SEG42	2278.6	316.5
133	SEG41	2248.4	316.5
134	SEG40	2218.2	316.5
135	SEG39	2188	316.5
136	SEG38	2157.8	316.5
137	SEG37	2127.6	316.5
138	SEG36	2097.4	316.5
139	SEG35	2067.2	316.5
140	SEG34	2037	316.5
141	SEG33	2006.8	316.5
142	SEG32	1976.6	316.5
143	SEG31	1946.4	316.5
144	SEG30	1916.2	316.5
145	SEG29	1886	316.5
146	SEG28	1855.8	316.5
147	SEG27	1825.6	316.5
148	SEG26	1795.4	316.5
149	SEG25	1765.2	316.5
150	SEG24	1735	316.5
151	SEG23	1704.8	316.5
152	SEG22	1674.6	316.5
153	SEG21	1644.4	316.5
154	SEG20	1614.2	316.5
155	SEG19	1584	316.5
156	SEG18	1553.8	316.5
157	SEG17	1523.6	316.5
158	SEG16	1493.4	316.5
159	SEG15	1463.2	316.5
160	SEG14	1433	316.5
161	SEG13	1402.8	316.5
162	SEG12	1372.6	316.5
163	SEG11	1342.4	316.5
164	SEG10	1312.2	316.5
165	SEG9	1282	316.5
166	SEG8	1251.8	316.5
167	SEG7	1221.6	316.5
168	SEG6	1191.4	316.5
169	SEG5	1161.2	316.5
170	SEG4	1131	316.5
171	SEG3	1100.8	316.5
172	SEG2	1070.6	316.5
173	SEG1	1040.4	316.5
174	SEG0	1010.2	316.5
175	VCC	980	316.5
176	VCC	949.8	316.5
177	VCC	919.6	316.5
178	VCC	889.4	316.5
179	VCOMH	840	300
180	VCOMH	800	300
181	COM0	760	300
182	COM1	720	300
183	COM2	680	300
184	COM3	640	300
185	COM4	600	300
186	COM5	560	300
187	COM6	520	300
188	COM7	480	300
189	COM8	440	300
190	COM9	400	300
191	COM10	360	300
192	COM11	320	300
193	COM12	280	300
194	COM13	240	300
195	COM14	200	300
196	COM15	160	300
197	COM16	120	300
198	COM17	80	300
199	COM18	40	300
200	COM19	0	300
201	COM20	-40	300
202	COM21	-80	300
203	COM22	-120	300
204	COM23	-160	300
205	COM24	-200	300
206	COM25	-240	300
207	COM26	-280	300
208	COM27	-320	300
209	COM28	-360	300
210	COM29	-400	300
211	COM30	-440	300
212	COM31	-480	300
213	COM32	-520	300
214	COM33	-560	300
215	COM34	-600	300
216	COM35	-640	300
217	COM36	-680	300
218	COM37	-720	300
219	COM38	-760	300
220	VCOMH	-800	300
221	VCOMH	-840	300
222	VCC	-889.4	316.5
223	VCC	-919.6	316.5
224	VCC	-949.8	316.5
225	VCC	-980	316.5
226	SEG64	-1010.2	316.5
227	SEG65	-1040.4	316.5
228	SEG66	-1070.6	316.5
229	SEG67	-1100.8	316.5
230	SEG68	-1131	316.5
231	SEG69	-1161.2	316.5
232	SEG70	-1191.4	316.5
233	SEG71	-1221.6	316.5
234	SEG72	-1251.8	316.5
235	SEG73	-1282	316.5
236	SEG74	-1312.2	316.5
237	SEG75	-1342.4	316.5
238	SEG76	-1372.6	316.5
239	SEG77	-1402.8	316.5
240	SEG78	-1433	316.5
241	SEG79	-1463.2	316.5
242	SEG80	-1493.4	316.5
243	SEG81	-1523.6	316.5
244	SEG82	-1553.8	316.5
245	SEG83	-1584	316.5
246	SEG84	-1614.2	316.5
247	SEG85	-1644.4	316.5
248	SEG86	-1674.6	316.5
249	SEG87	-1704.8	316.5
250	SEG88	-1735	316.5
251	SEG89	-1765.2	316.5
252	SEG90	-1795.4	316.5
253	SEG91	-1825.6	316.5
254	SEG92	-1855.8	316.5
255	SEG93	-1886	316.5
256	SEG94	-1916.2	316.5
257	SEG95	-1946.4	316.5
258	SEG96	-1976.6	316.5
259	SEG97	-2006.8	316.5
260	SEG98	-2037	316.5
261	SEG99	-2067.2	316.5
262	SEG100	-2097.4	316.5
263	SEG101	-2127.6	316.5
264	SEG102	-2157.8	316.5
265	SEG103	-2188	316.5
266	SEG104	-2218.2	316.5
267	SEG105	-2248.4	316.5
268	SEG106	-2278.6	316.5
269	SEG107	-2308.8	316.5
270	SEG108	-2339	316.5
271	SEG109	-2369.2	316.5
272	SEG110	-2399.4	316.5
273	SEG111	-2429.6	316.5
274	SEG112	-2459.8	316.5
275	SEG113	-2490	316.5
276	SEG114	-2520.2	316.5
277	SEG115	-2550.4	316.5
278	SEG116	-2580.6	316.5
279	SEG117	-2610.8	316.5
280	SEG118	-2641	316.5
281	SEG119	-2671.2	316.5
282	SEG120	-2701.4	316.5
283	SEG121	-2731.6	316.5
284	SEG122	-2761.8	316.5
285	SEG123	-2792	316.5
286	SEG124	-2822.2	316.5
287	SEG125	-2852.4	316.5
288	SEG126	-2882.6	316.5
289	SEG127	-2912.8	316.5
290	VCC	-2943	316.5
291	VCC	-2973.2	316.5
292	VCC	-3003.4	316.5
293	NC	-2986.4	6.575
294	NC	-2986.4	-33.425
295	NC	-2986.4	-73.425
296	NC	-2986.4	-113.425
297	NC	-2986.4	-153.425
298	NC	-2986.4	-193.425

6 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 6-1 : Pin Description

Pin Name	Type	Description
V_{DD}	P	Power supply pin for core logic operation.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{SS}	P	This is a ground pin.
V_{LSS}	P	This is an analog ground pin. It should be connected to V_{SS} externally.
V_{COMH}	O	The pin is for COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}. When external V_{COMH} is selected, this pin must be connected to V_{CC}. Refer to command ADh for details.
V_{BAT}	P	Power supply for charge pump regulator circuit. Status / V_{BAT} / V_{DD} / V_{CC} Enable charge pump / Connect to external V_{BAT} source / Connect to external V_{DD} source / A capacitor should be connected between this pin and V_{SS} Disable charge pump / Keep float / Connect to external V_{DD} source / Connect to external V_{CC} source
BGGND	P	Reserved pin. It should be connected to V_{SS} externally.
C1P/C1N C2P/C2N	O	C1P/C1N – Pin for charge pump capacitor; Connect to each other with a capacitor. C2P/C2N – Pin for charge pump capacitor; Connect to each other with a capacitor.
V_{BREF}	O	Reserved pin. It should be kept NC.
BS[2:0]	I	MCU bus interface selection pins. Please refer to Table 6-2 for the details of setting.
I_{REF}	I	This is segment output current reference pin. When external I_{REF} is used, a resistor should be connected between this pin and V_{SS} to maintain the I_{REF} current at 10uA. Please refer to Figure 7-14 for the details of resistor value. When internal I_{REF} is used, this pin should be kept NC.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.

Pin Name	Type	Description
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V_{DD}) during normal operation.
CS#	I	This pin is the chip select input. (active LOW)
D/C#	I	This is Data/Command control pin. When it is pulled HIGH (i.e. connect to V_{DD}), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V_{DD}) and the chip is selected. When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin must be connected to V_{SS}.
R/W#(WR#)	I	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V_{DD}) and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	IO	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
GPIO0/GPIO1	IO	Reserved pin. It should be kept NC.
TR[9:0]	IO	Reserved pin. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide Segment switch signals to OLED panel. These pins are V_{SS} state when display is OFF.
COM0 ~ COM38	O	These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.
NC	-	This is dummy pin. Do not group or short NC pins together.

Table 6-2 : MCU Bus Interface Pin Selection

SSD1316 Pin Name	I^2C Interface	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0	0	0	1
BS1	1	0	1	0	0
BS2	0	1	1	0	0

Note

(1) 0 is connected to V_{SS}

(2) 1 is connected to V_{DD}

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface selection

SSD1316 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 7-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 6-2 for BS[2:0] setting).

Table 7-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

7.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

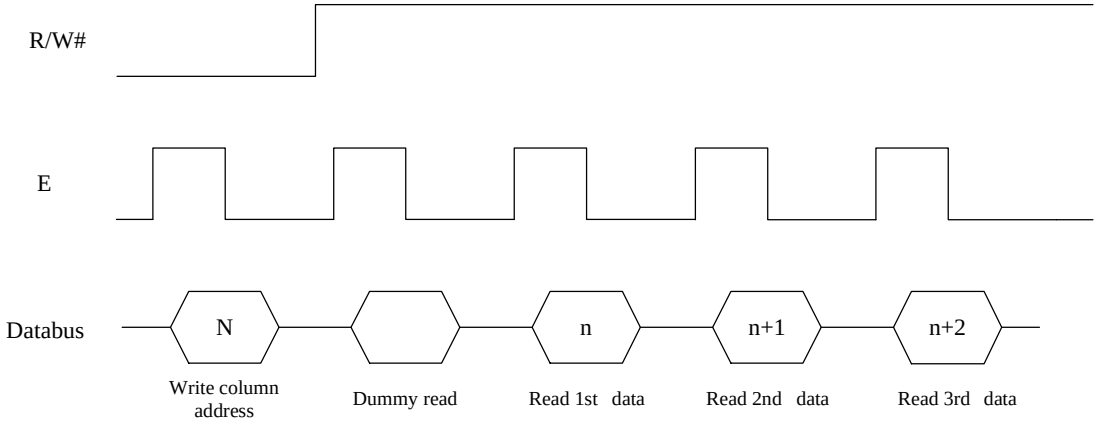
Table 7-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1 : Data read back procedure - insertion of dummy read



7.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2 : Example of Write procedure in 8080 parallel interface mode

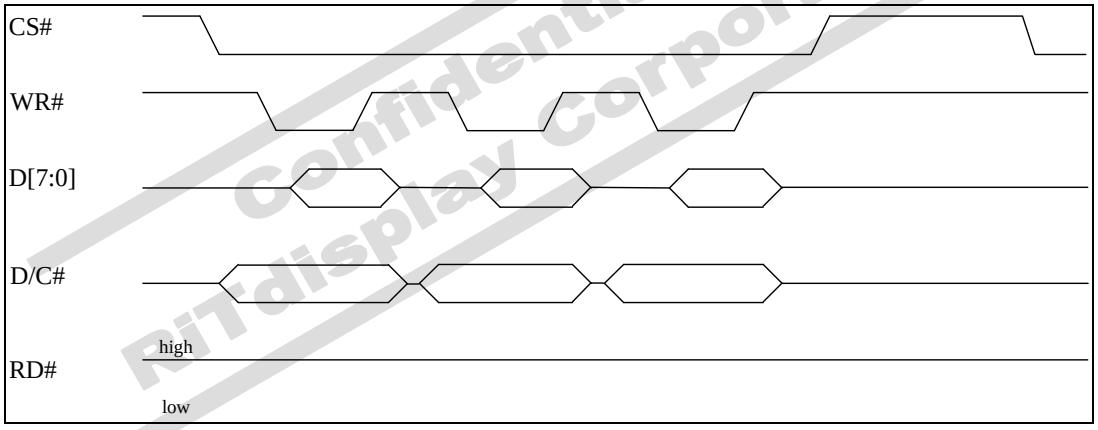


Figure 7-3 : Example of Read procedure in 8080 parallel interface mode

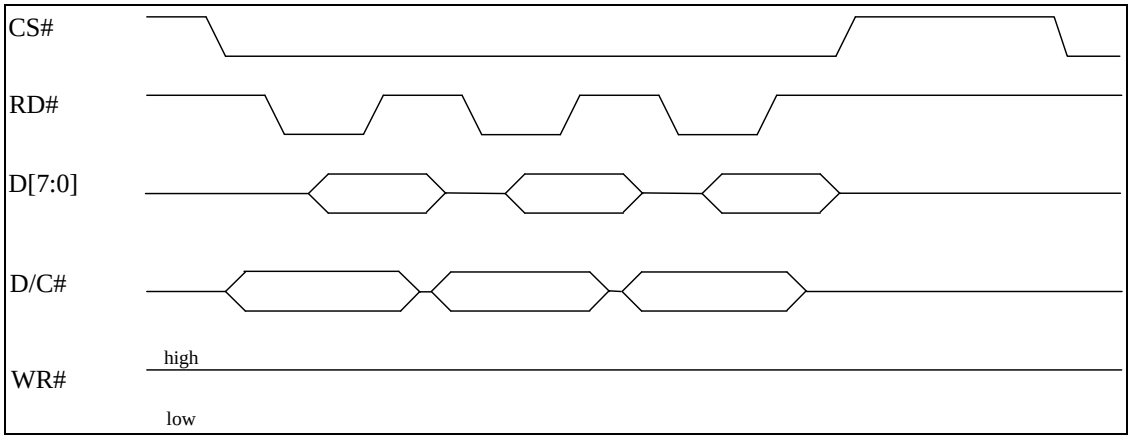


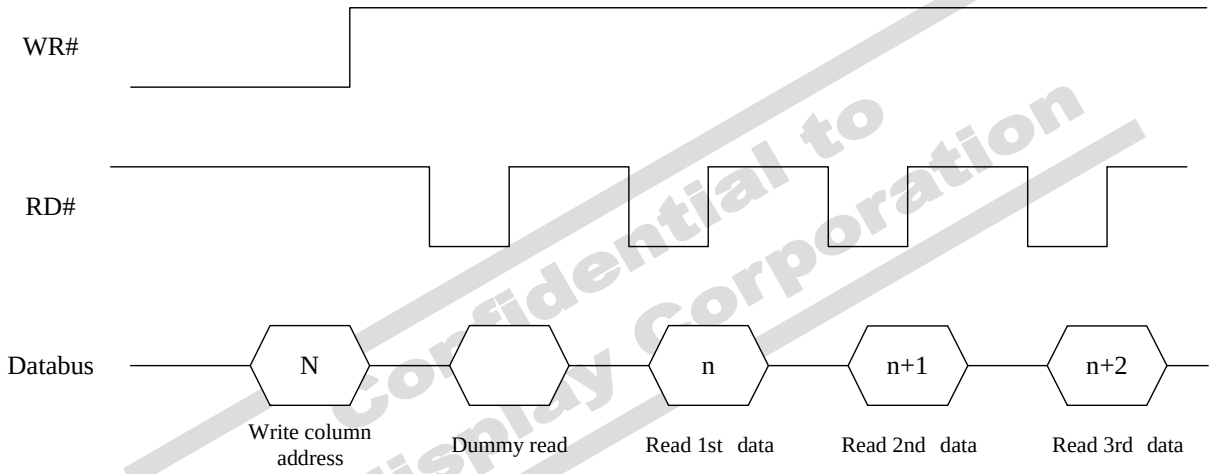
Table 7-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4 : Display data read back procedure - insertion of dummy read



7.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

Table 7-4 : Control pins of 4-wire Serial interface

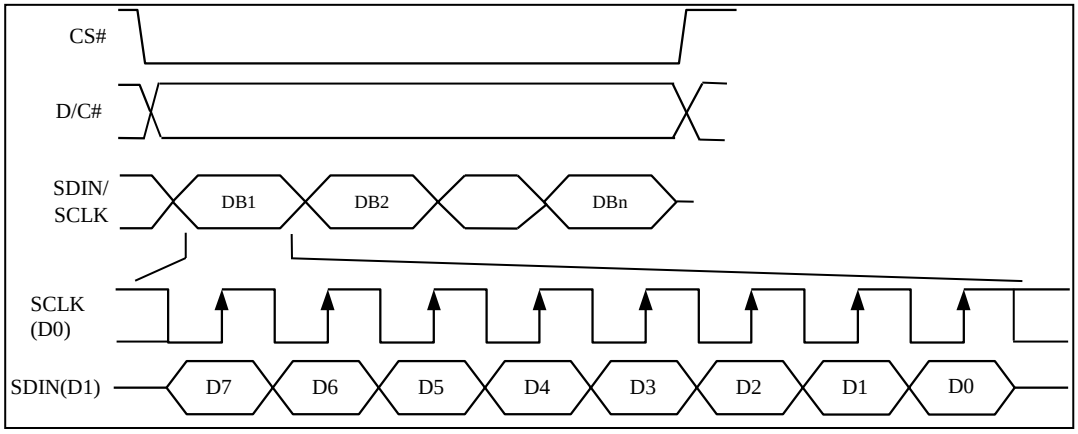
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 7-5 : Write procedure in 4-wire Serial interface mode



7.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

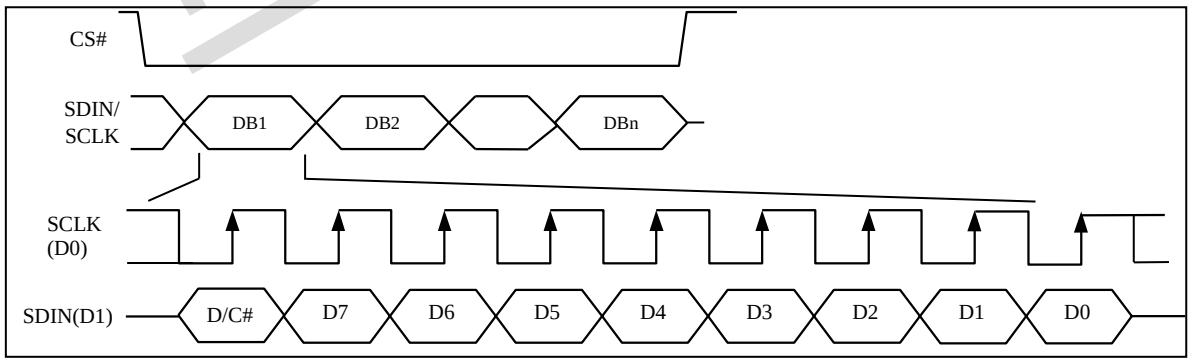
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 7-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 7-6 : Write procedure in 3-wire Serial interface mode



7.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1316 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1316. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

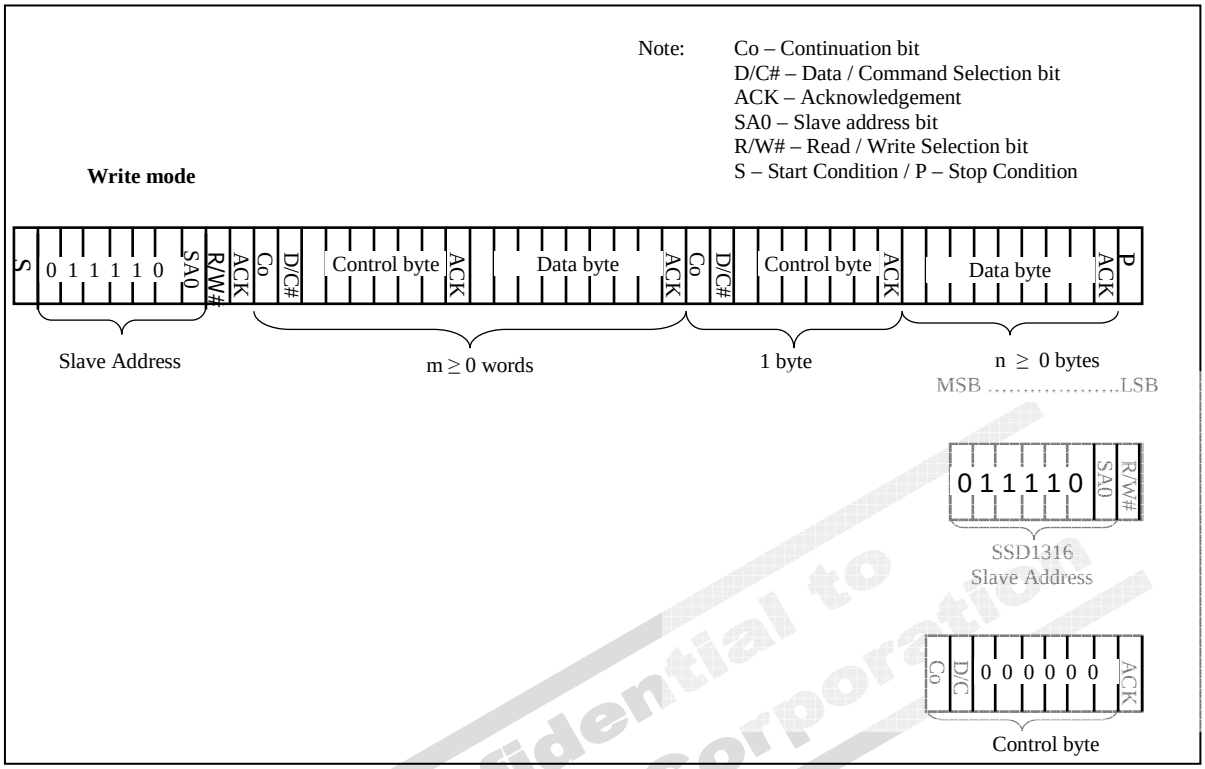
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

7.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 7-7 for the write mode of I²C-bus in chronological order.

Figure 7-7 : I²C-bus data format



7.1.5.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1316, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 7-8 : Definition of the Start and Stop Condition

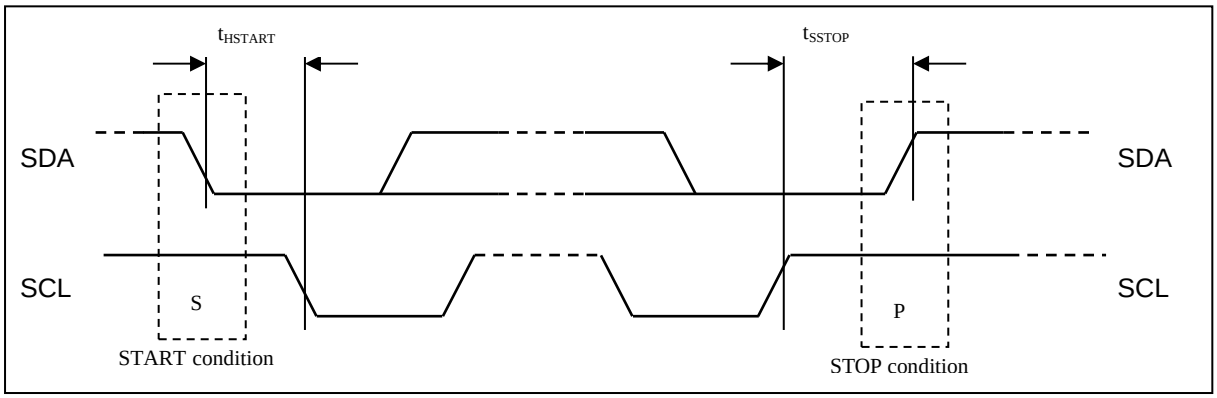
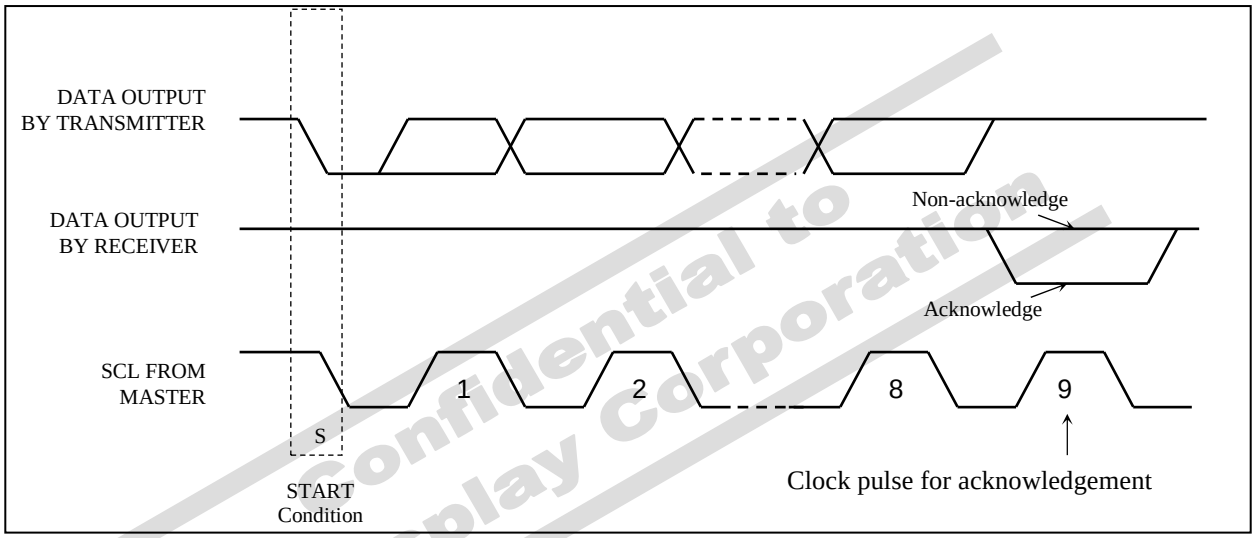


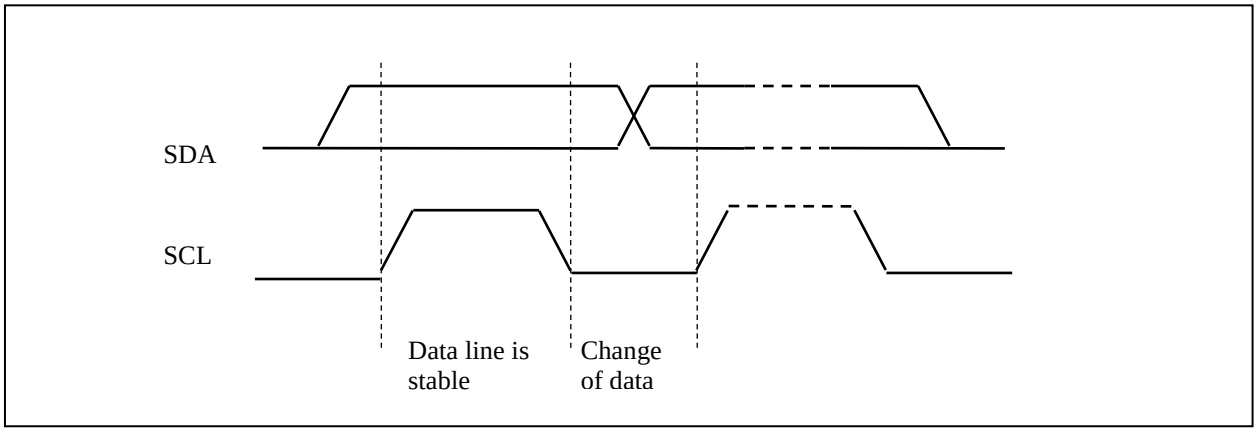
Figure 7-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 7-10 : Definition of the data transfer condition



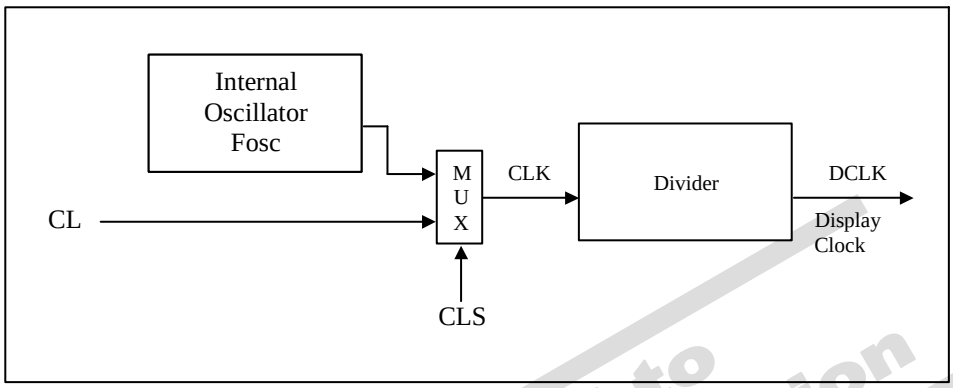
7.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

7.3 Oscillator Circuit and Display Time Generator

Figure 7-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

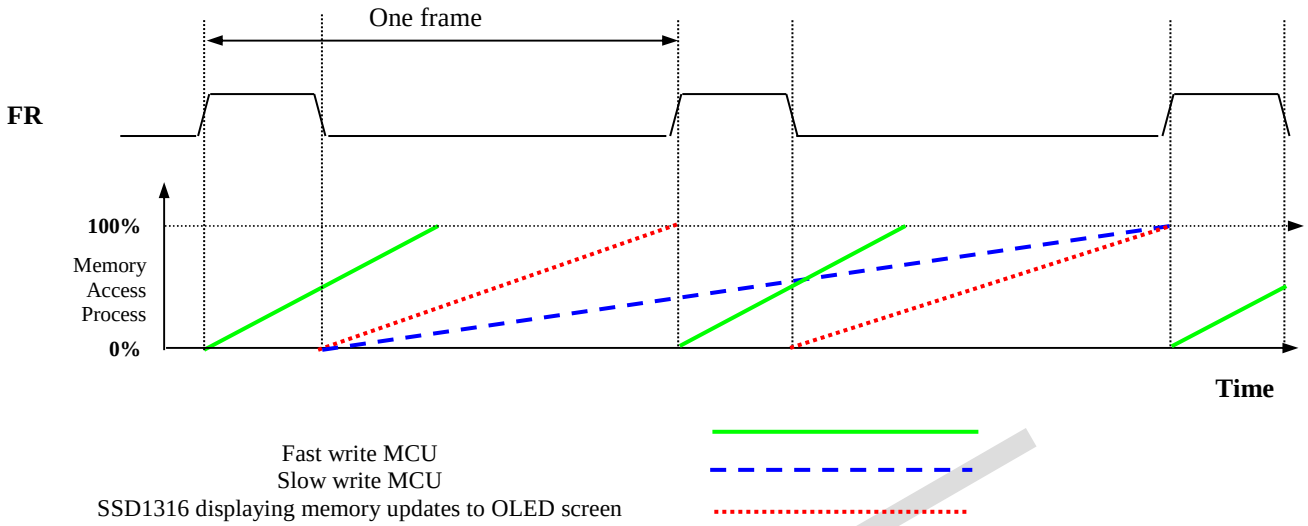
$$F_{FRM} = \frac{F_{osc}}{D \times K \times No.\ of\ Mux}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 2 + 2 + 50 = 54 at power on reset (that is K_o is a constant that equals to 50)
  (Please refer to Section 7.6 for the details of the "Phase")
- Number of multiplex ratio is set by command A8h. The power on reset value is 38 (i.e. 39MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

7.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

7.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 39 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

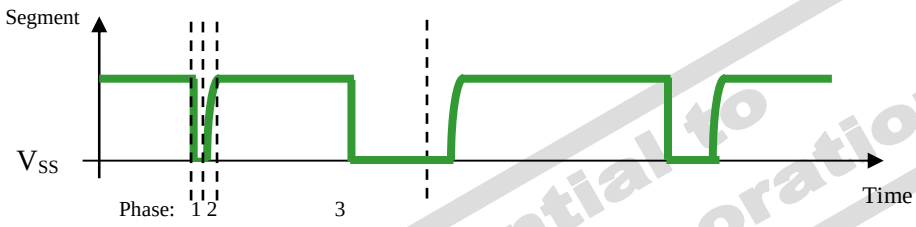
7.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted by altering the registers of the contrast setting command (81h). Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 7-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 50, after finishing 50 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

7.7 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 39 bits and the RAM is divided into five pages, from PAGE0 to PAGE4, which are used for monochrome 128 x 39 dot matrix display, as shown in Figure 7-13.

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row. For PAGE4, bit D7 is treated as don't care bit.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.
For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

Figure 7-13 : GDDRAM pages structure of SSD1316

Segment re-mapping (command A1h)		SEG127	SEG126	SEG125	SEG124	.....	SEG4	SEG3	SEG2	SEG1	SEG0		
Segment re-mapping (command A0h [RESET])		SEG0	SEG1	SEG2	SEG3	.....	SEG123	SEG124	SEG125	SEG126	SEG127		
Page	Data	COL0	COL1	COL2	COL3	.....	COL123	COL124	COL125	COL126	COL127	COM Output Scan Direction (command C0h [RESET])	COM Output Scan Direction (command C8h)
0	D0					.....						COM0	COM38
	D1											COM1	COM37
	D2											COM2	COM36
	D3											COM3	COM35
	D4											COM4	COM34
	D5											COM5	COM33
	D6											COM6	COM32
	D7											COM7	COM31
1	D0					.....						COM8	COM30
	D1											COM9	COM29
	D2											COM10	COM28
	D3											COM11	COM27
	D4											COM12	COM26
	D5											COM13	COM25
	D6											COM14	COM24
	D7											COM15	COM23
2	D0					.....						COM16	COM22
	D1											COM17	COM21
	D2											COM18	COM20
	D3											COM19	COM19
	D4											COM20	COM18
	D5											COM21	COM17
	D6											COM22	COM16
	D7											COM23	COM15
3	D0					.....						COM24	COM14
	D1											COM25	COM13
	D2											COM26	COM12
	D3											COM27	COM11
	D4											COM28	COM10
	D5											COM29	COM9
	D6											COM30	COM8
	D7											COM31	COM7
4	D0					.....						COM32	COM6
	D1											COM33	COM5
	D2											COM34	COM4
	D3											COM35	COM3
	D4											COM36	COM2
	D5											COM37	COM1
	D6											COM38	COM0
	D7	Don't care bit											

Each box represents one bit of image data

7.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{LSS} is the ground path of the analog and panel current.
- V_{COMH} is the Common deselected level. It can be internally regulated or externally connect to $V_{CC.}$

  Bit A[1] of command ADh is used to select external or internal V_{COMH}:
  A[1] = '0' Select external V_{COMH}. When external V_{COMH} is used, V_{COMH} must be connected to V_{CC}.
  A[1] = '1' Select internal V_{COMH} regulator [Reset]. When internal V_{COMH} is selected, a capacitor should be connected between V_{COMH} and $V_{SS.}$

- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

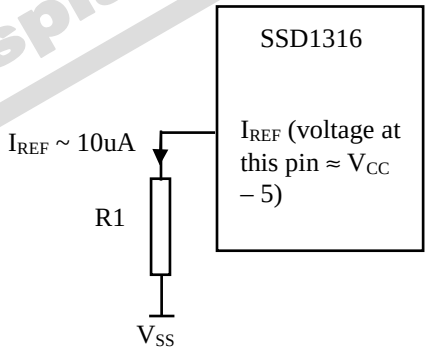
  I_{SEG} = Contrast / 256 x I_{REF} x scale factor

  in which the contrast (1~255) is set by Set Contrast command (81h)

  When internal I_{REF} is used, the I_{REF} pin should be kept NC.
  Bit A[4] of command ADh is used to select external or internal I_{REF} :
  A[4] = '0' Select external I_{REF} [Reset]
  A[4] = '1' Enable internal I_{REF} during display ON

When external I_{REF} is used, the magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and VSS as shown in Figure 7-14. It is recommended to set I_{REF} to 10 ± 2uA so as to achieve I_{SEG} = 160uA at maximum contrast 255.

Figure 7-14 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 5V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 5) / 10uA
= 700kΩ

7.9 Power ON and OFF sequence

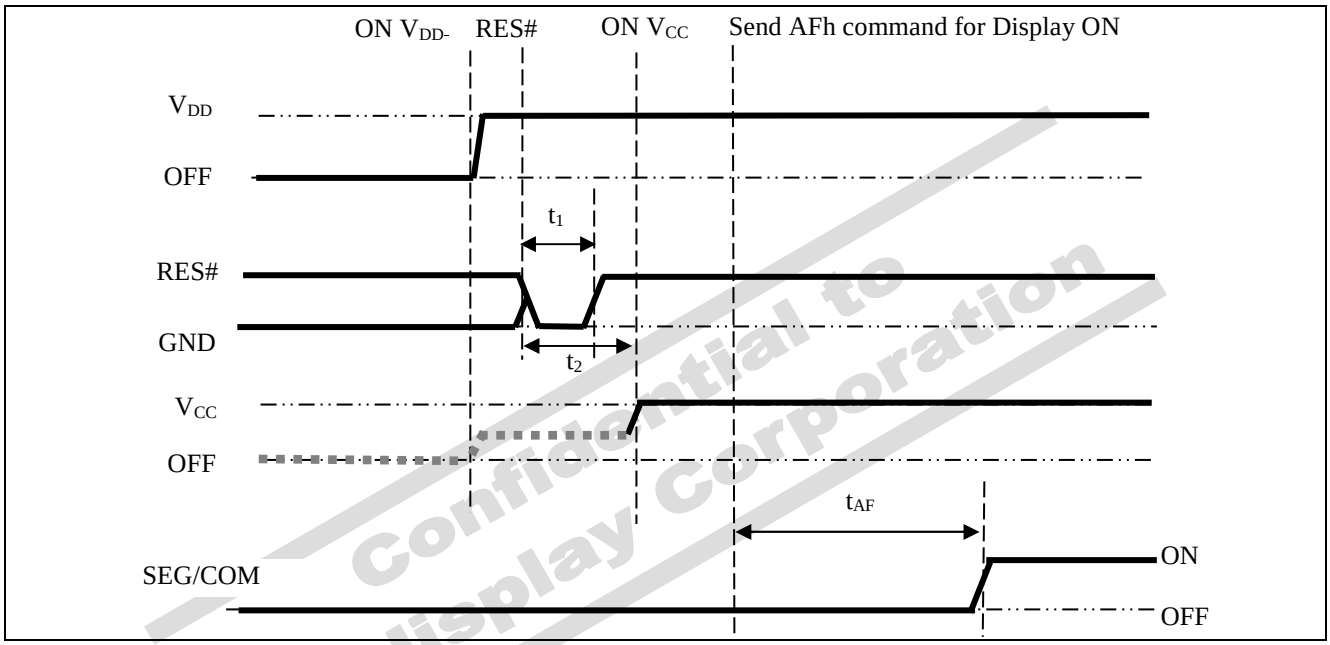
The following figures illustrate the recommended power ON and power OFF sequence of SSD1316 :

7.9.1 Power ON and OFF sequence with External V_{CC}

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

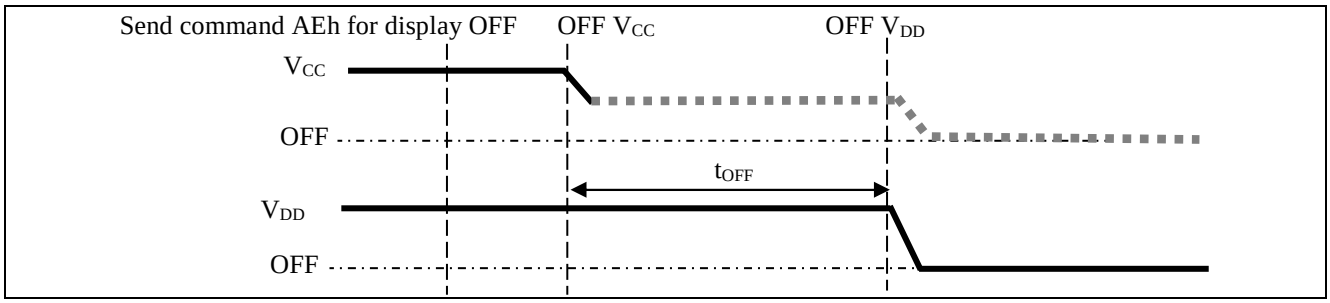
Figure 7-15 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. [1], [2], [3]
3. Power OFF V_{DD} after t_{OFF}. [5] (Typical t_{OFF}=500ms)

Figure 7-16 : The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-15 and Figure 7-16.

[2] V_{CC} should be kept float (i.e. disable) when it is OFF.

[3] Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

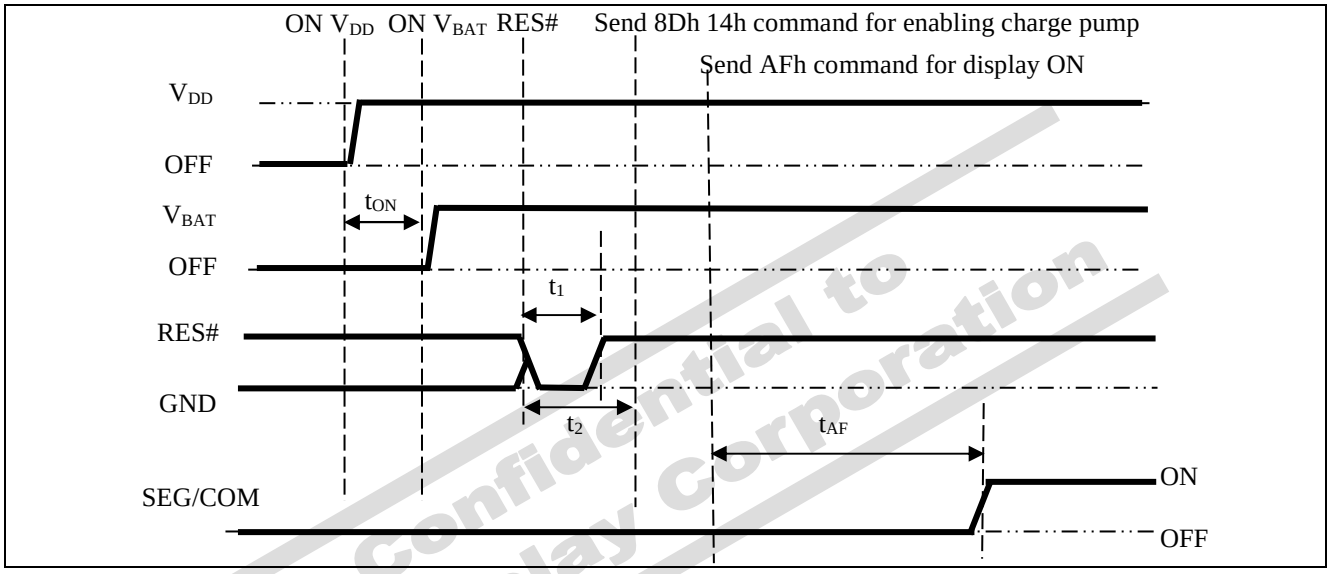
[5] V_{DD} should not be Power OFF before V_{CC} Power OFF.

7.9.2 Power ON and OFF sequence with Charge Pump Application

Power ON sequence:

1. Power ON V_{DD}
2. Wait for t_{ON}. Power ON V_{BAT}.[1, 2] (where Minimum t_{ON} = 0ms)
3. After V_{BAT} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [3] and then HIGH (logic high).
4. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then input commands with below sequence:
   a. 8Dh 14h for enabling charge pump
   b. AFh for display ON
5. SEG/COM will be ON after 100ms (t_{AF}).

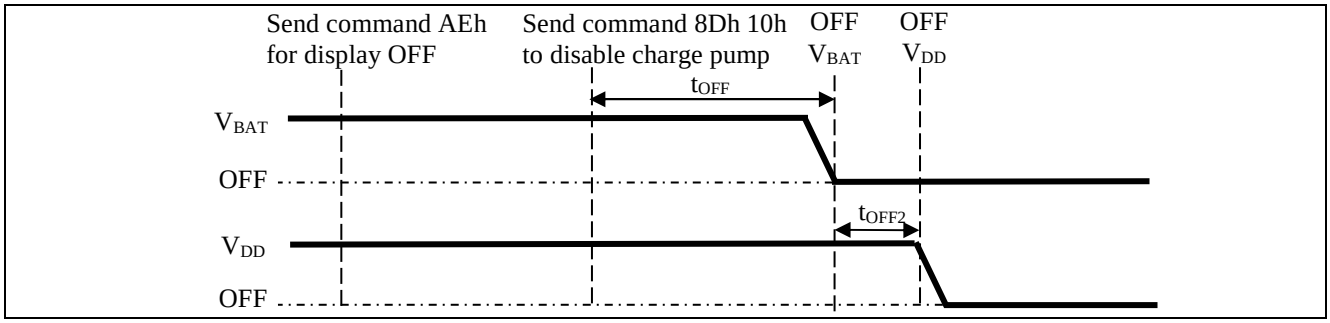
Figure 7-17 : The Power ON sequence with Charge Pump Application



Power OFF sequence:

1. Send command AEh for display OFF
2. Send command 8Dh 10h to disable charge pump
3. Power OFF V_{BAT} after t_{OFF}. .[1, 2] (Typical t_{OFF} =500ms)
4. Power OFF V_{DD} after t_{OFF2}. (where Minimum t_{OFF2} = 0ms [4] , Typical t_{OFF2}=5ms)

Figure 7-18 : The Power OFF sequence with Charge Pump Application



Note:

[1] V_{BAT} should be kept float (i.e. disable) when it is OFF.
[2] Power Pins (V_{DD} , V_{BAT}) can never be pulled to ground under any circumstance.
[3] The register values are reset after t_1.
[4] V_{DD} should not be Power OFF before V_{BAT} Power OFF

7.10 Charge Pump Regulator

The internal regulator circuit in SSD1316 accompanying only 2 external capacitors can generate a 9.0V voltage supply, V_{CC} and a maximum output loading of 12mA from a low voltage supply input, V_{BAT}. The V_{CC} is the voltage supply to the OLED driver block. This regulator can be turned ON/OFF by software command 8Dh setting.

8 COMMAND TABLE

Table 8-1: SSD1316 Command Table

(R/W#(WR#) = 0, E(RD#) = 1 unless specific setting is stated)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select one of the contrast steps. Contrast increases as the value increases. (RESET = 7Fh) A[7:0] valid range: 01h to FFh
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X[0]: Resume to RAM content display (RESET) Output follows RAM content A5h, X[0]: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	AD A[7:0]	1 0	0 0	1 0	0 A_4	1 0	1 0	0 A_1	1 0	External or Internal V_{COMH} Selection / External or internal I_{REF} Selection	Select external or internal V_{COMH} : A[1] = '0' Select internal V_{COMH} (RESET) A[1] = '1' Enable external V_{COMH} Select external or internal I_{REF} : A[4] = '0' Select external I_{REF} (RESET) A[4] = '1' Enable internal I_{REF} during display ON **Note** (1) Refer to section 7.8 for details.
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – invalid 001b – PAGE1 | 100b – PAGE4 | 111b – invalid 010b – PAGE2 | 101b – invalid | C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 5 frame 011b – 128 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – invalid 001b – PAGE1 | 100b – PAGE4 | 111b – invalid 010b – PAGE2 | 101b – invalid | The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Define start column address (00d-127d) G[7:0] : Define end column address (00d-127d) The value of G[2:0] must be larger or equal to F[2:0]
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	0	0	0	0		
0	F[7:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[7:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll A[7:0] : Horizontal scrolling offset A[0] = 0, no offset A[0] = 1, scroll by 1 column
0	A[2:0]	*	*	*	*	*	*	*	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[7:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[7:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0		

2. Scrolling Command Table

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>B[2:0] : Define start page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – invalid</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – invalid</td></tr><tr><td>010b – PAGE2</td><td>101b – invalid</td><td></td></tr></table>
C[2:0] : Set time interval between each scroll step in terms of frame frequency
<table><tr><td>000b – 6 frames</td><td>100b – 3 frames</td></tr><tr><td>001b – 32 frames</td><td>101b – 4 frames</td></tr><tr><td>010b – 64 frames</td><td>110b – 5 frame</td></tr><tr><td>011b – 128 frames</td><td>111b – 2 frame</td></tr></table>
D[2:0] : Define end page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – invalid</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – invalid</td></tr><tr><td>010b – PAGE2</td><td>101b – invalid</td><td></td></tr></table>The value of D[2:0] must be larger or equal to B[2:0]

E[5:0] : Vertical scrolling offset
e.g. E[5:0]= 01h refer to offset =1 row
E[5:0] =26h refer to offset =38 rows

F[7:0] : Define start column address (00d-127d)

G[7:0] : Define end column address (00d-127d)
The value of G[2:0] must be larger or equal to F[2:0]</td></tr>
<tr><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Deactivate scroll</td><td>Stop scrolling that is configured by command 26h/27h/29h/2Ah.

Note
(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.</td></tr>
</table>

2. Scrolling Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[5:0] B[5:0]	1 * *	0 * *	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0d] B[5:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 39d] **Note** (1) A[5:0]+B[5:0] <= MUX ratio (2) B[5:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[5:0] (3b) Set Display Start Line (X5X4X3X2X1X0 of 40h~66h) < B[5:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 39d MUX display A[5:0] = 0, B[5:0]=39 : whole area scrolls A[5:0]= 0, B[5:0] < 39 : top area scrolls A[5:0] + B[5:0] < 39 : central area scrolls A[5:0] + B[5:0] = 39 : bottom area scrolls

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2C/2D	0	0	1	0	1	1	0	X_0	Content Scroll Setup	2Ch, X[0]=0, Right Horizontal Scroll by one column 2Dh, X[0]=1, Left Horizontal Scroll by one column A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – invalid 001b – PAGE1 | 100b – PAGE4 | 111b – invalid 010b – PAGE2 | 101b – invalid | C[7:0] : Dummy byte (Set as 01h) D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – invalid 001b – PAGE1 | 100b – PAGE4 | 111b – invalid 010b – PAGE2 | 101b – invalid | E[7:0] : Dummy byte (Set as 00h) F[7:0] : Define start column (RESET = 00h) G[7:0] : Define end column (RESET = 7Fh) **Note** (1) The value of D[2:0] must be larger than or equal to B[2:0] (2) The value of G[7:0] must be larger than F[7:0] (3) A delay time of 2 frame frequency must be set if sending the command of 2Ch / 2Dh consecutively
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[7:0]	*	*	*	*	*	0	0	1		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	0	0	0	0		
0	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[7:0]	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		

3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode.

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	10~17	0	0	0	1	0	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[2:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode.
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-4d, (RESET = 0d) B[2:0] : Page end Address, range : 0-4d, (RESET = 4d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	B0~B4	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE4) for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode.

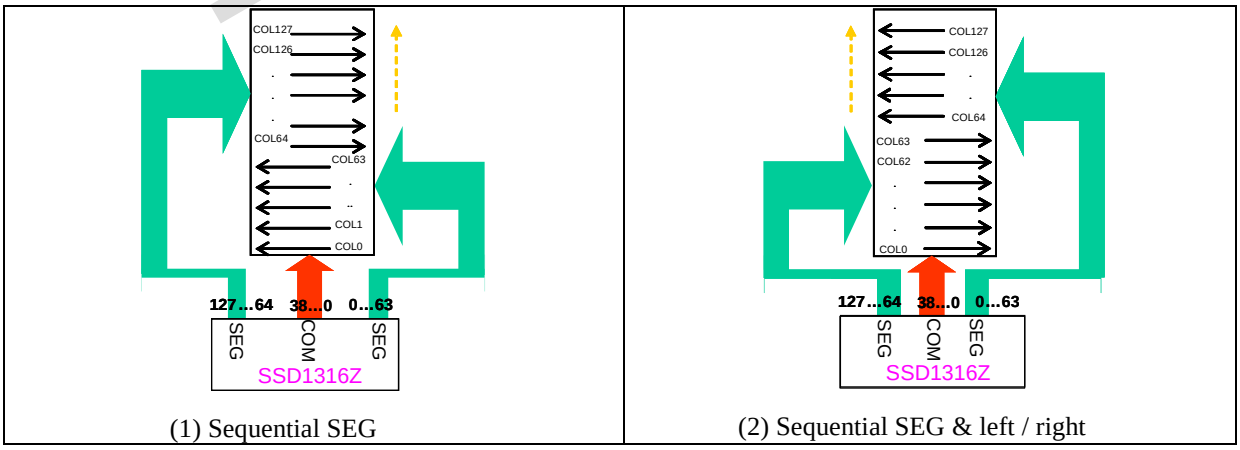
4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~66	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display offset from 0d-38d using $X_5X_4X_3X_2X_1X_0$. Display offset is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0

4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 8MUX to 39MUX, RESET= 100110b (i.e.38d , 39Mux) A[5:0] from 0 to 7 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~38d. The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set SEG Pins Hardware Configuration	A[4]=0b, Sequential SEG pin configuration A[4]=1b(RESET), Alternative (odd/even) SEG pin configuration A[5]=0b(RESET), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap

Table 8-2 : SEG Pins Hardware Configuration

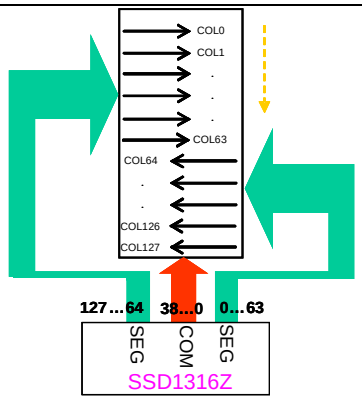
SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings,

Case no.	Oddeven (1) / Sequential (0) Command : DAh -> A[4]	SEG Remap Command : A0h / A1h	Left / Right Swap Command : DAh -> A[5]	Remark
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	Default
6	1	0	1	
7	1	1	0	
8	1	1	1	

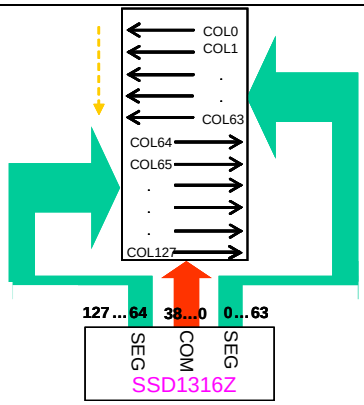


(1) Sequential SEG

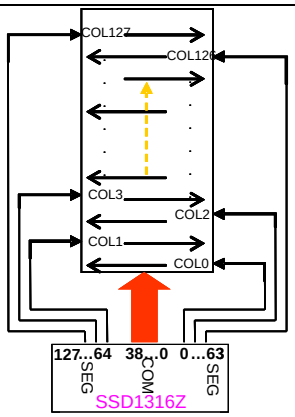
(2) Sequential SEG & left / right



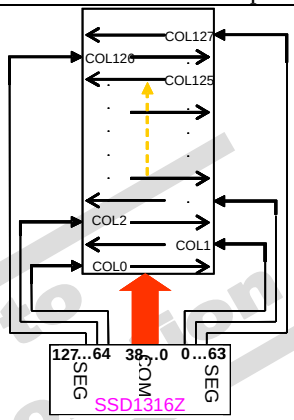
(3) Sequential SEG & SEG remap



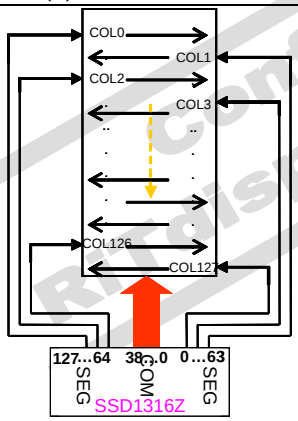
(4) Sequential SEG & SEG remap & left / right



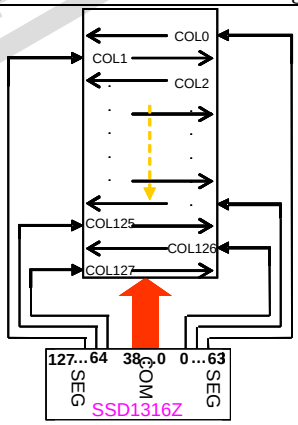
(5) Odd / even SEG



(6) Odd / even SEG & left / right



(7) Odd / even SEG & SEG remap



(8) Odd / even SEG & SEG remap & left / right

Note:

(1) The above eight figures are all with bump pads being faced up.

5. Timing & Driving scheme Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0001b (divide ratio = 2) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1100b Range:0000b~1111b Frequency increases as setting value increases.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks. 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks .0 is invalid entry (RESET=2h)
0 0	DB A[6:4]	1 0	1 A_6	0 A_5	1 A_4	1 0	0 0	1 0	1 0	Set V_{COMH} Deselect Level	A[6:4] / Hex code / V_{COMH} deselect level 000b / 00h / ~ 0.65 x V_{CC} 010b / 20h / ~ 0.77 x V_{CC} (RESET) 011b / 30h / ~ 0.83 x V_{CC}

<table>
<tr><th colspan="12">6. Advance Graphic Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0</td><td>23
A[6:0]</td><td>0
*</td><td>0
*</td><td>1
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Fade Out and Blinking</td><td>A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET]

A[5:4] = 01b Enable Fade In mode.
Once Fade In Mode is enabled, contrast increase gradually to original contrast setting. Output follows RAM content when Fade mode is disabled.

A[5:4] = 10b Enable Fade Out mode.
Once Fade Out Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled.

A[5:4] = 11b Enable Blinking mode.
Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and than contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled.

A[3:0] : Set time interval for each fade step

<table><tr><td>A[3:0]</td><td>Time interval for each fade step</td></tr><tr><td>0000b</td><td>8 Frames</td></tr><tr><td>0001b</td><td>16 Frames</td></tr><tr><td>0010b</td><td>24 Frames</td></tr><tr><td colspan="2">:</td></tr><tr><td>1111b</td><td>128 Frames</td></tr></table>
Note
(1) Refer to section 9.3.1 for details.</td></tr>
<tr><td>0
0</td><td>D6
A[0]</td><td>1
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>1
0</td><td>0
A0</td><td>Set Zoom In</td><td>A[0] = 0b Disable Zoom in Mode[RESET]
A[0] = 1b Enable Zoom in Mode

Note
(1) The panel must be in alternative COM pin configuration (command DAh A[4] =1)
(2) Refer to section 9.3.2 for details.</td></tr>
</table>

7. Charge Pump Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	8D	1	0	0	0	1	1	0	1	Charge Pump Setting	A[0] = 0b, Select 9V charge pump output (RESET) A[0] = 1b, Select 7.5V charge pump output A[2] = 0b, Disable charge pump(RESET) A[2] = 1b, Enable charge pump during display on **Note** (1) The Charge Pump must be enabled by the following command sequence: 8Dh ; Charge Pump Setting 14h / 15h ; Enable Charge Pump AFh; Display ON
0	A[7:0]	*	*	0	1	0	A_2	0	A_0		

8. Others											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

Note

(1) "*" stands for "Don't care".

Table 8-3 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : "1" for display OFF / "0" for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note

(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

8.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 8-4 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command

9.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 8-1 and Section 9.1.3 for details.

9.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~17h)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 8-1 and Section 9.1.3 for details.

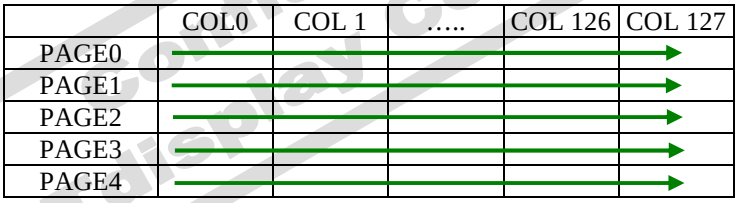
9.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1316: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, "COL" means the graphic display data RAM column.

Page addressing mode (A[1:0]=10xb)

In page addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 9-1.

Figure 9-1 : Address Pointer Movement of Page addressing mode

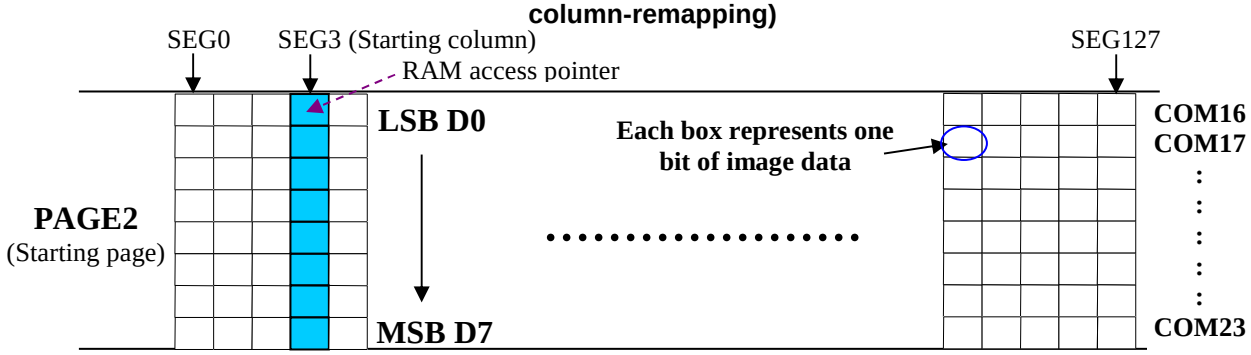


In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B4h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~17h.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 9-2. The input data byte will be written into RAM position of column 3.

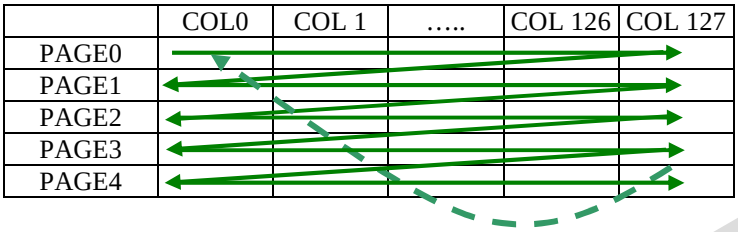
Figure 9-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



Horizontal addressing mode (A[1:0]=00b)

In horizontal addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 9-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 9-3.)

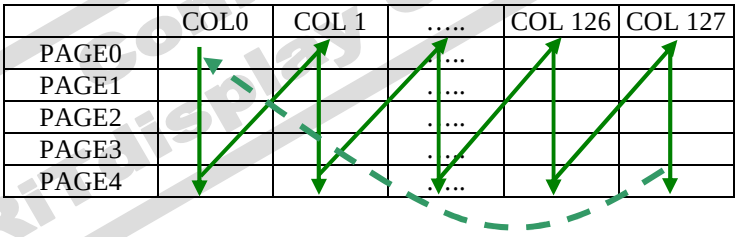
Figure 9-3 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (A[1:0]=01b)

In vertical addressing mode, after the display RAM is read / written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 9-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 9-4.)

Figure 9-4 : Address Pointer Movement of Vertical addressing mode



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 9-5.

9.1.4 Set Column Address (21h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

9.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 97, page start address is set to 1 and page end address is set to 2; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 97 and from page 1 to page 2 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 9-5*). Whenever the column address pointer finishes accessing the end column 97, it is reset back to column 2 and page address is automatically increased by 1 (*solid line in Figure 9-5*). While the end page 2 and end column 97 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line in Figure 9-5*). .

Figure 9-5 : Example of Column and Row Address Pointer Movement

	Col 0	Col 1	Col 2	…..	…….	Col 97	Col98	.....	Col 126	Col 127
PAGE0										
PAGE1										
PAGE2										
PAGE3										
PAGE4										

9.1.6 Set Display Start Line (40h~66h)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 38. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

Refer to Table 9-1 for more illustrations.

9.1.7 Set Contrast Control (81h)

This command sets the Contrast Setting of the display, with a valid range from 01h to FFh. The segment output current increases as the contrast step value increases.

9.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 8-2.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

9.1.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.
In other words, A4h command resumes the display from entire display "ON" stage.
A5h command forces the entire display to be "ON", regardless of the contents of the display data RAM.

9.1.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an "ON" pixel while in inverse display a RAM data of 0 indicates an "ON" pixel.

9.1.11 Set Multiplex Ratio (A8h)

This command switches the default 39 multiplex mode to any multiplex ratio, ranging from 8 to 39. The output pads COM0~COM38 will be switched to the corresponding COM signal.

9.1.12 External or Internal VCOMH Selection / External or internal IREF Selection (ADh)

This double byte command consists of two functions:

- External or Internal V_{COMH} Selection (A[1])
  When A[1] = '0', Select external V_{COMH}. When external V_{COMH} is selected, the V_{COMH} pin must be connected to V_{CC}.
  Default A[1] = '1', Select internal V_{COMH}

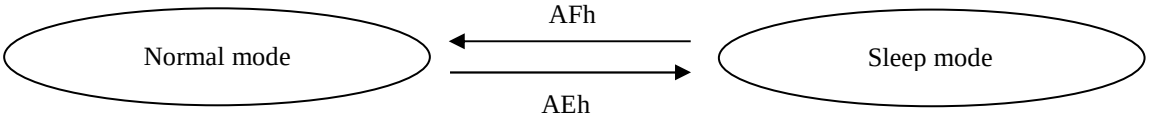
- External or Internal I_{REF} Selection (A[4])
  Default A[4] = '0', Select external I_{REF}.
  When A[4] = '1', Select internal I_{REF} during display ON. Refer to Section 7.8 for details.

9.1.13 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 9-6 : Transition between different modes



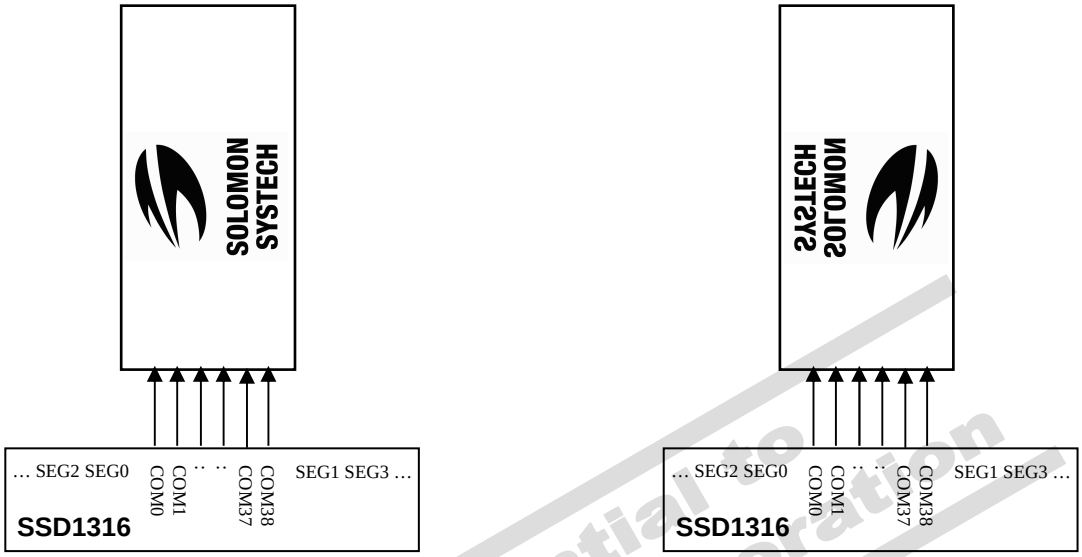
9.1.14 Set Page Start Address for Page Addressing Mode (B0h~B4h)

This command positions the page start address from 0 to 4 in GDDRAM under Page Addressing Mode. Please refer to Table 8-1 and Section 9.1.3 for details.

9.1.15 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display, then the graphic display will be vertically flipped immediately. Please refer to Figure 9-7 and Table 9-2 for details.

Figure 9-7 : Example of row address mapping



Row 0 maps to COM0 pin

Row 38 maps to COM0 pin

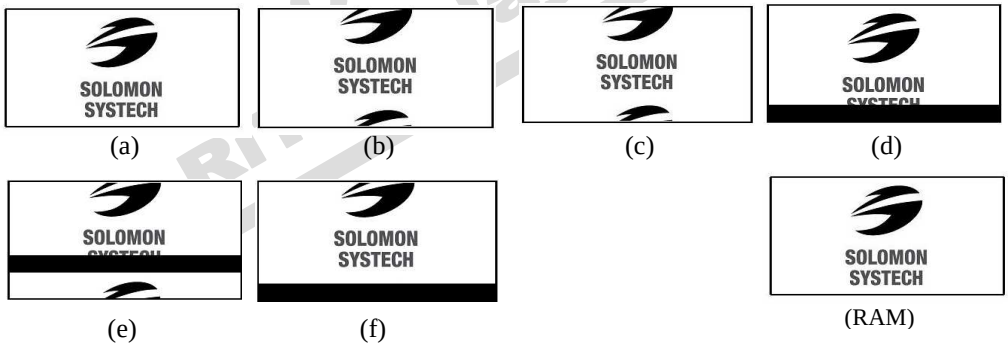
9.1.16 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM38 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM4 towards the COM0 direction by 4 lines the 6-bit data in the second byte should be given as 000100b. To move in the opposite direction by 4 lines the 6-bit data should be given by 39 – 4, so the second byte would be 100011b. The following two tables (Table 9-1, Table 9-2) show the examples of setting the command C0h/C8h and D3h.

Table 9-1 : Example of Set Display Offset and Display Start Line without Remap

	Output												
	39		39		39		32		32		32		Set MUX ration (A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM normal / remap (C0h / C8h)
Hardware	0		4		0		0		4		0		Display offset (D3h)
pin name	0		0		4		0		0		4		Display start line (40h - 66h)
COM0	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	
COM1	ROW1	RAM1	ROW5	RAM5	ROW1	RAM5	ROW1	RAM1	ROW5	RAM5	ROW1	RAM5	
COM2	ROW2	RAM2	ROW6	RAM6	ROW2	RAM6	ROW2	RAM2	ROW6	RAM6	ROW2	RAM6	
COM3	ROW3	RAM3	ROW7	RAM7	ROW3	RAM7	ROW3	RAM3	ROW7	RAM7	ROW3	RAM7	
COM4	ROW4	RAM4	ROW8	RAM8	ROW4	RAM8	ROW4	RAM4	ROW8	RAM8	ROW4	RAM8	
COM5	ROW5	RAM5	ROW9	RAM9	ROW5	RAM9	ROW5	RAM5	ROW9	RAM9	ROW5	RAM9	
COM6	ROW6	RAM6	ROW10	RAM10	ROW6	RAM10	ROW6	RAM6	ROW10	RAM10	ROW6	RAM10	
COM7	ROW7	RAM7	ROW11	RAM11	ROW7	RAM11	ROW7	RAM7	ROW11	RAM11	ROW7	RAM11	
COM8	ROW8	RAM8	ROW12	RAM12	ROW8	RAM12	ROW8	RAM8	ROW12	RAM12	ROW8	RAM12	
COM9	ROW9	RAM9	ROW13	RAM13	ROW9	RAM13	ROW9	RAM9	ROW13	RAM13	ROW9	RAM13	
COM10	ROW10	RAM10	ROW14	RAM14	ROW10	RAM14	ROW10	RAM10	ROW14	RAM14	ROW10	RAM14	
COM11	ROW11	RAM11	ROW15	RAM15	ROW11	RAM15	ROW11	RAM11	ROW15	RAM15	ROW11	RAM15	
COM12	ROW12	RAM12	ROW16	RAM16	ROW12	RAM16	ROW12	RAM12	ROW16	RAM16	ROW12	RAM16	
COM13	ROW13	RAM13	ROW17	RAM17	ROW13	RAM17	ROW13	RAM13	ROW17	RAM17	ROW13	RAM17	
COM14	ROW14	RAM14	ROW18	RAM18	ROW14	RAM18	ROW14	RAM14	ROW18	RAM18	ROW14	RAM18	
COM15	ROW15	RAM15	ROW19	RAM19	ROW15	RAM19	ROW15	RAM15	ROW19	RAM19	ROW15	RAM19	
COM16	ROW16	RAM16	ROW20	RAM20	ROW16	RAM20	ROW16	RAM16	ROW20	RAM20	ROW16	RAM20	
COM17	ROW17	RAM17	ROW21	RAM21	ROW17	RAM21	ROW17	RAM17	ROW21	RAM21	ROW17	RAM21	
COM18	ROW18	RAM18	ROW22	RAM22	ROW18	RAM22	ROW18	RAM18	ROW22	RAM22	ROW18	RAM22	
COM19	ROW19	RAM19	ROW23	RAM23	ROW19	RAM23	ROW19	RAM19	ROW23	RAM23	ROW19	RAM23	
COM20	ROW20	RAM20	ROW24	RAM24	ROW20	RAM24	ROW20	RAM20	ROW24	RAM24	ROW20	RAM24	
COM21	ROW21	RAM21	ROW25	RAM25	ROW21	RAM25	ROW21	RAM21	ROW25	RAM25	ROW21	RAM25	
COM22	ROW22	RAM22	ROW26	RAM26	ROW22	RAM26	ROW22	RAM22	ROW26	RAM26	ROW22	RAM26	
COM23	ROW23	RAM23	ROW27	RAM27	ROW23	RAM27	ROW23	RAM23	ROW27	RAM27	ROW23	RAM27	
COM24	ROW24	RAM24	ROW28	RAM28	ROW24	RAM28	ROW24	RAM24	ROW28	RAM28	ROW24	RAM28	
COM25	ROW25	RAM25	ROW29	RAM29	ROW25	RAM29	ROW25	RAM25	ROW29	RAM29	ROW25	RAM29	
COM26	ROW26	RAM26	ROW30	RAM30	ROW26	RAM30	ROW26	RAM26	ROW30	RAM30	ROW26	RAM30	
COM27	ROW27	RAM27	ROW31	RAM31	ROW27	RAM31	ROW27	RAM27	ROW31	RAM31	ROW27	RAM31	
COM28	ROW28	RAM28	ROW32	RAM32	ROW28	RAM32	ROW28	RAM28	-	-	ROW28	RAM32	
COM29	ROW29	RAM29	ROW33	RAM33	ROW29	RAM33	ROW29	RAM29	-	-	ROW29	RAM33	
COM30	ROW30	RAM30	ROW34	RAM34	ROW30	RAM34	ROW30	RAM30	-	-	ROW30	RAM34	
COM31	ROW31	RAM31	ROW35	RAM35	ROW31	RAM35	ROW31	RAM31	-	-	ROW31	RAM35	
COM32	ROW32	RAM32	ROW36	RAM36	ROW32	RAM36	-	-	-	-	-	-	
COM33	ROW33	RAM33	ROW37	RAM37	ROW33	RAM37	-	-	-	-	-	-	
COM34	ROW34	RAM34	ROW38	RAM38	ROW34	RAM38	-	-	-	-	-	-	
COM35	ROW35	RAM35	ROW0	RAM0	ROW35	RAM0	-	-	ROW0	RAM0	-	-	
COM36	ROW36	RAM36	ROW1	RAM1	ROW36	RAM1	-	-	ROW1	RAM1	-	-	
COM37	ROW37	RAM37	ROW2	RAM2	ROW37	RAM2	-	-	ROW2	RAM2	-	-	
COM38	ROW38	RAM38	ROW3	RAM3	ROW38	RAM3	-	-	ROW3	RAM3	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		

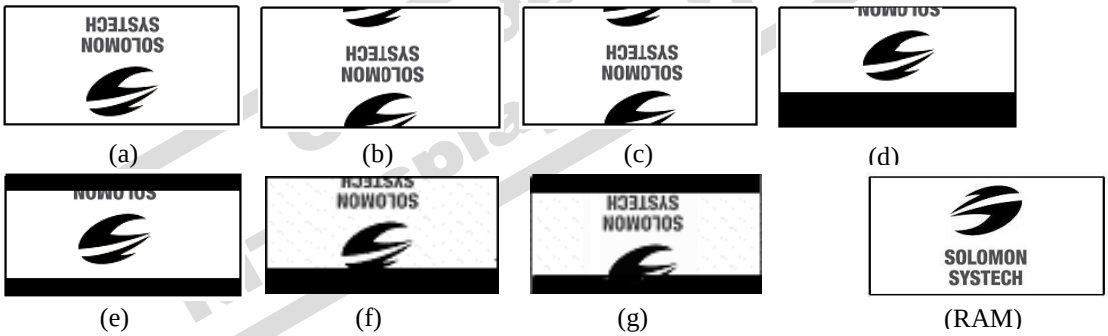


(a) (b) (c) (d)

(e) (f) (RAM)

Table 9-2 : Example of Set Display Offset and Display Start Line with Remap

	Output														
	39		39		39		32		32		32		32		Set MUX ration (A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM normal / remap (C0h / C8h)
Hardware	0		4		0		0		4		0		4		Display offset (D3h)
pin name	0		0		4		0		0		4		8		Display start line (40h - 66h)
COM0	ROW38	RAM 38	ROW3	RAM3	ROW38	RAM3	ROW31	RAM31	-	-	ROW31	RAM35	-	-	
COM1	ROW37	RAM37	ROW2	RAM2	ROW37	RAM2	ROW30	RAM30	-	-	ROW30	RAM34	-	-	
COM2	ROW36	RAM36	ROW1	RAM1	ROW36	RAM1	ROW29	RAM29	-	-	ROW29	RAM33	-	-	
COM3	ROW35	RAM35	ROW0	RAM0	ROW35	RAM0	ROW28	RAM28	-	-	ROW28	RAM32	-	-	
COM4	ROW34	RAM34	ROW38	RAM38	ROW34	RAM38	ROW27	RAM27	ROW31	RAM31	ROW27	RAM31	ROW31	RAM0	
COM5	ROW33	RAM33	RAM37	RAM37	ROW33	RAM37	ROW26	RAM26	ROW30	RAM30	ROW26	RAM30	ROW30	RAM38	
COM6	ROW32	RAM32	RAM36	RAM36	ROW32	RAM36	ROW25	RAM25	ROW29	RAM29	ROW25	RAM29	ROW29	RAM37	
COM7	ROW31	RAM31	RAM35	RAM35	ROW31	RAM35	ROW24	RAM24	ROW28	RAM28	ROW24	RAM28	ROW28	RAM36	
COM8	ROW30	RAM30	RAM34	RAM34	ROW30	RAM34	ROW23	RAM23	ROW27	RAM27	ROW23	RAM27	ROW27	RAM35	
COM9	ROW29	RAM29	RAM33	RAM33	ROW29	RAM33	ROW22	RAM22	ROW26	RAM26	ROW22	RAM26	ROW26	RAM34	
COM10	ROW28	RAM28	RAM32	RAM32	ROW28	RAM32	ROW21	RAM21	ROW25	RAM25	ROW21	RAM25	ROW25	RAM33	
COM11	ROW27	RAM27	RAM31	RAM31	ROW27	RAM31	ROW20	RAM20	ROW24	RAM24	ROW20	RAM24	ROW24	RAM32	
COM12	ROW26	RAM26	RAM30	RAM30	ROW26	RAM30	ROW19	RAM19	ROW23	RAM23	ROW19	RAM23	ROW23	RAM31	
COM13	ROW25	RAM25	RAM29	RAM29	ROW25	RAM29	ROW18	RAM18	ROW22	RAM22	ROW18	RAM22	ROW22	RAM30	
COM14	ROW24	RAM24	RAM28	RAM28	ROW24	RAM28	ROW17	RAM17	ROW21	RAM21	ROW17	RAM21	ROW21	RAM29	
COM15	ROW23	RAM23	RAM27	RAM27	ROW23	RAM27	ROW16	RAM16	ROW20	RAM20	ROW16	RAM20	ROW20	RAM28	
COM16	ROW22	RAM22	RAM26	RAM26	ROW22	RAM26	ROW15	RAM15	ROW19	RAM19	ROW15	RAM19	ROW19	RAM27	
COM17	ROW21	RAM21	RAM25	RAM25	ROW21	RAM25	ROW14	RAM14	ROW18	RAM18	ROW14	RAM18	ROW18	RAM26	
COM18	ROW20	RAM20	RAM24	RAM24	ROW20	RAM24	ROW13	RAM13	ROW17	RAM17	ROW13	RAM17	ROW17	RAM25	
COM19	ROW19	RAM19	RAM23	RAM23	ROW19	RAM23	ROW12	RAM12	ROW16	RAM16	ROW12	RAM16	ROW16	RAM24	
COM20	ROW18	RAM18	RAM22	RAM22	ROW18	RAM22	ROW11	RAM11	ROW15	RAM15	ROW11	RAM15	ROW15	RAM23	
COM21	ROW17	RAM17	RAM21	RAM21	ROW17	RAM21	ROW10	RAM10	ROW14	RAM14	ROW10	RAM14	ROW14	RAM22	
COM22	ROW16	RAM16	RAM20	RAM20	ROW16	RAM20	ROW9	RAM9	ROW13	RAM13	ROW9	RAM13	ROW13	RAM21	
COM23	ROW15	RAM15	RAM19	RAM19	ROW15	RAM19	ROW8	RAM8	ROW12	RAM12	ROW8	RAM12	ROW12	RAM20	
COM24	ROW14	RAM14	RAM18	RAM18	ROW14	RAM18	ROW7	RAM7	ROW11	RAM11	ROW7	RAM11	ROW11	RAM19	
COM25	ROW13	RAM13	RAM17	RAM17	ROW13	RAM17	ROW6	RAM6	ROW10	RAM10	ROW6	RAM10	ROW10	RAM18	
COM26	ROW12	RAM12	RAM16	RAM16	ROW12	RAM16	ROW5	RAM5	ROW9	RAM9	ROW5	RAM9	ROW9	RAM17	
COM27	ROW11	RAM11	RAM15	RAM15	ROW11	RAM15	ROW4	RAM4	ROW8	RAM8	ROW4	RAM8	ROW8	RAM16	
COM28	ROW10	RAM10	RAM14	RAM14	ROW10	RAM14	ROW3	RAM3	ROW7	RAM7	ROW3	RAM7	ROW7	RAM15	
COM29	ROW9	RAM9	RAM13	RAM13	ROW9	RAM13	ROW2	RAM2	ROW6	RAM6	ROW2	RAM6	ROW6	RAM14	
COM30	ROW8	RAM8	RAM12	RAM12	ROW8	RAM12	ROW1	RAM1	ROW5	RAM5	ROW1	RAM5	ROW5	RAM13	
COM31	ROW7	RAM7	RAM11	RAM11	ROW7	RAM11	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	ROW4	RAM12	
COM32	ROW6	RAM6	RAM10	RAM10	ROW6	RAM10	-	-	ROW3	RAM3	-	-	ROW3	RAM11	
COM33	ROW5	RAM5	RAM9	RAM9	ROW5	RAM9	-	-	ROW2	RAM2	-	-	ROW2	RAM10	
COM34	ROW4	RAM4	RAM8	RAM8	ROW4	RAM8	-	-	ROW1	RAM1	-	-	ROW1	RAM9	
COM35	ROW3	RAM3	RAM7	RAM7	ROW3	RAM7	-	-	ROW0	RAM0	-	-	ROW0	RAM8	
COM36	ROW2	RAM2	RAM6	RAM6	ROW2	RAM6	-	-	-	-	-	-	-	-	
COM37	ROW1	RAM1	RAM5	RAM5	ROW1	RAM5	-	-	-	-	-	-	-	-	
COM38	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



(a) (b) (c) (d)

(e) (f) (g) (RAM)

9.1.17 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 0001b. Please refer to section 7.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1100b.

9.1.18 Set Pre-charge Period (D9h)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals to 2 DCLKs.

9.1.19 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. Table 8-2 shows the COM pin configuration under different conditions (for MUX ratio = 39).

9.1.20 Set V_{COMH} Deselect Level (DBh)

This command adjusts the VCOMH regulator output.

9.1.21 NOP (E3h)

No Operation Command

9.1.22 Status register Read

This command is issued by setting D/C# ON LOW during a data read (See Figure 12-1 to Figure 12-2 for parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

9.1.23 Charge Pump Setting (8Dh)

This command controls the ON/OFF of the Charge Pump. The Charge Pump must be enabled by the following command sequence:

8Dh ; Charge Pump Setting
14h or 15h; Enable Charge Pump at selectable 9V mode or 7.5V mode
AFh; Display ON

9.2 Graphic Acceleration Command

9.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of 7 consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page, start column, end column and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1316 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 9-8, Figure 9-9, and Figure 9-10) show the examples of using the horizontal scroll:

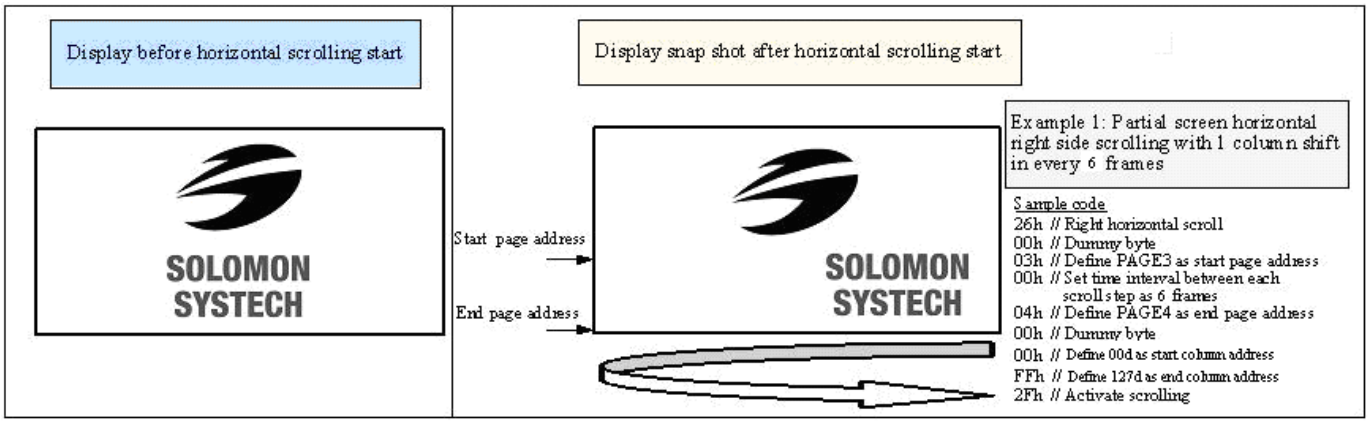
Figure 9-8 : Horizontal scroll example: Scroll RIGHT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	…	…	…	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG127	SEG0	SEG1	SEG2	SEG3	SEG4	…	…	…	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126

Figure 9-9 : Horizontal scroll example: Scroll LEFT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	…	…	…	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	…	…	SEG123	SEG124	SEG125	SEG126	SEG127	SEG0

Figure 9-10 : Horizontal scrolling setup example



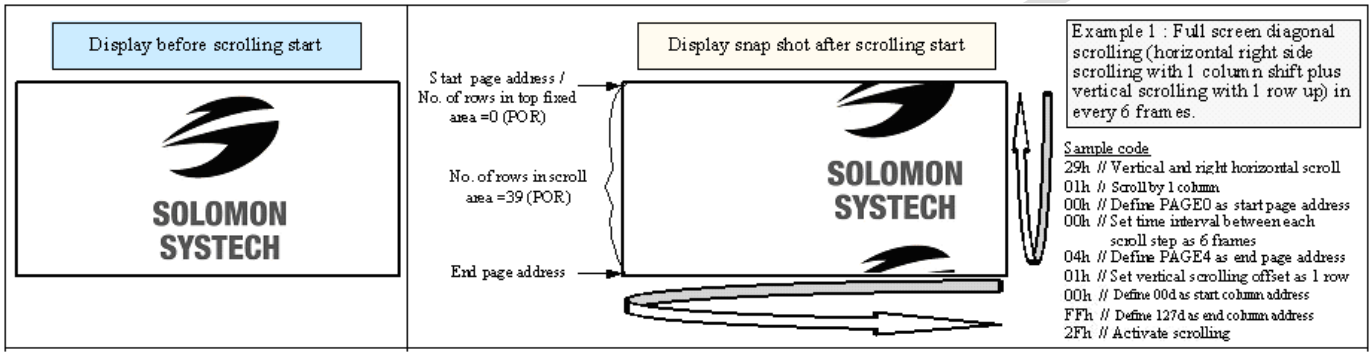
9.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of 7 consecutive bytes to set up the continuous vertical scroll parameters and determines the scrolling start page, end page, start column, end column, scrolling speed, horizontal and vertical scrolling offset.

The bytes A[0], B[2:0], C[2:0], D[2:0], E[5:0], F[6:0] and G[6:0] of command 29h/2Ah are for the setting of the continuous horizontal scrolling. The byte E[5:0] is for the setting of the continuous vertical scrolling offset. All these bytes together are for the setting of continuous diagonal (horizontal + vertical) scrolling. If the vertical scrolling offset byte E[5:0] is set to zero, then only horizontal scrolling is performed (like command 26/27h).

Before issuing this command the scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted. The following figure (Figure 9-11) show the example of using the continuous vertical and horizontal scroll:

Figure 9-11 : Continuous Vertical and Horizontal scrolling setup example



9.2.3 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

9.2.4 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands: 26h / 27h / 29h / 2Ah. The setting in the latest scrolling setup command overwrites the setting in the previous scrolling setup command.

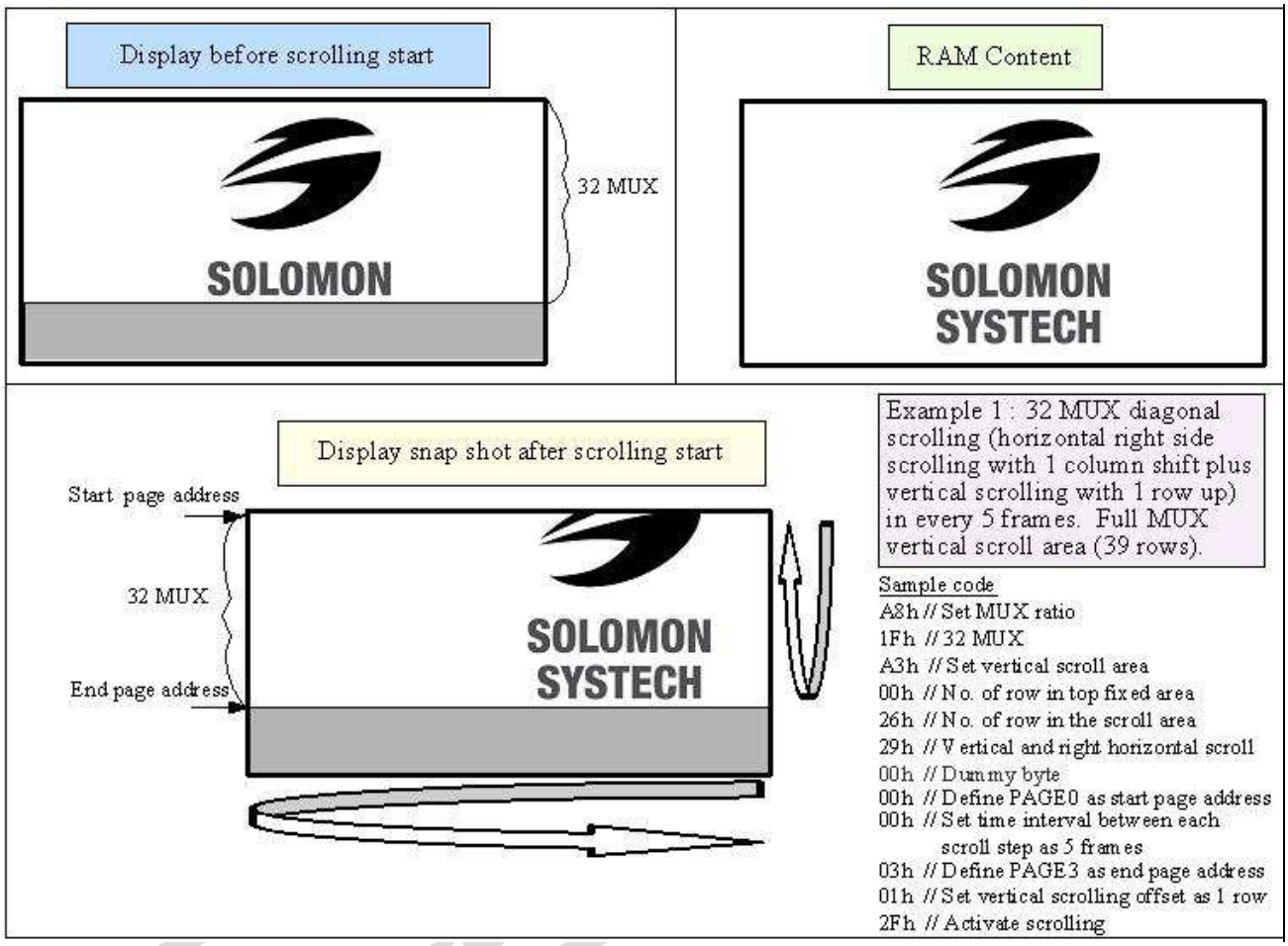
The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

9.2.5 Set Vertical Scroll Area (A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29h / 2Ah), the number of rows in the vertical scroll area can be set smaller than or equating to the MUX ratio. Figure 9-12 shows some vertical scrolling example with different settings in vertical scroll area.

Figure 9-12 : Vertical scroll area setup examples

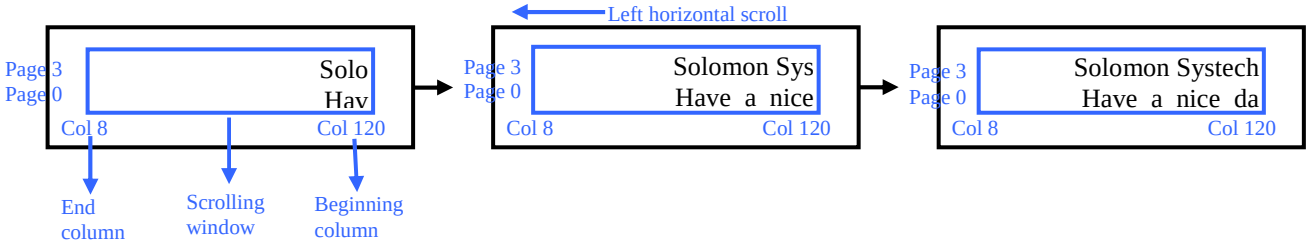


9.2.6 Content Scroll Setup (2Ch/2Dh)

This command consists of seven consecutive bytes to set up the horizontal scroll parameters and determine the scrolling start page, end page, start column and end column. One column will be scrolled horizontally by sending the setting of command 2Ch / 2Dh once.

When command 2Ch / 2Dh are sent consecutively, a delay time of Frame Frequency of 2 must be set. Figure 9-13 shown an example of using 2Dh “Content Scroll Setup” command for horizontal scrolling to left with infinite content update. In there, “Col” means the graphic display data RAM column.

Figure 9-13: Content Scrolling example (2Dh, Left Horizontal Scroll by one column)



By using command 2Ch/2Dh, RAM contents are scrolled and updated by one column. Table 9-3 is an example of content scrolling setting of SSD1316 (scrolling window of 4 pages). The values of registers depend on different conditions and applications.

Table 9-3 : Content Scrolling software flow example (Page addressing mode – command 20h, 02h)

Step	Action	D/C#	Code	Remarks
1	**For i= 1 to n**	-	-	Create "For loop" for infinite content scrolling
2	Set Content scrolling command (scrolling window : Page 0 to 3, Col 8 to Col 120)	0	2Dh	Left Horizontal Scroll by one column
		0	00h	A[7:0] : Dummy byte (Set as 00h)
		0	00h	B[2:0] : Define start page address
		0	01h	C[7:0] : Dummy byte (Set as 01h)
		0	03h	D[2:0] : Define end page address
		0	00h	E[7:0] : Dummy byte (Set as 00h)
		0	08h	F[6:0] : Define start column address
		0	78h	G[6:0] : Define end column address
3	Add Delay time of $2/FrameFreq$	-	-	E.g. Delay 20ms if frame freq ≈ 100Hz
4	Write RAM on the beginning column of the scrolling window			
	Write RAM on (Page0, Col 120) *(Content update in beginning column)*	0	B0h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page1, Col 120) *(Content update in beginning column)*	0	B1h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page2, Col 120) *(Content update in beginning column)*	0	B2h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page3, Col 120) *(Content update in beginning column)*	0	B3h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
5	i=i+1	-	-	Go to next "For loop"
	Delay timing	-	-	Set time interval between each scroll step if necessary
	End			

There are 3 different memory addressing mode in SSD1316: page addressing mode, horizontal addressing mode and vertical addressing mode and it is selected by command 20h. Table 9-3 is an example of content scrolling software flow under page addressing mode, while vertical addressing mode example is shown in below Table 9-4.

Table 9-4 : Content Scrolling setting example (Vertical addressing mode – command 20h, 01h)

Step	Action	D/C#	Code	Remarks
1	**For i= 1 to n**	-	-	Create "For loop" for infinite content scrolling
2	Set Content scrolling command (scrolling window : Page 0 to 3, Col 8 to Col 120)	0	2Dh	Left Horizontal Scroll by one column
		0	00h	A[6:0] : Dummy byte (Set as 00h)
		0	00h	B[2:0] : Define start page address
		0	01h	C[2:0] : Dummy byte (Set as 01h)
		0	03h	D[2:0] : Define end page address
		0	00h	E[6:0] : Dummy byte (Set as 00h)
		0	08h	F[6:0] : Define start column address
		0	78h	G[6:0] : Define end column address
3	Add Delay time of $2/FrameFreq$	-	-	E.g. Delay 20ms if frame freq ≈ 100Hz
4	Write RAM on the beginning column of the scrolling window (Page 0 to 3, Col 120) *(Content update in beginning column)*	0	21h	Set Column address
		0	78h	Set column start address for Vertical Addressing Mode
		0	78h	Set column end address for Vertical Addressing Mode
		0	22h	Set Page address
		0	00h	Set start page address for Vertical Addressing Mode
		0	03h	Set end page address for Vertical Addressing Mode
		1	-	Write data to fill the RAM
5	i=i+1	-	-	Go to next "For loop"
	Delay timing	-	-	Set time interval between each scroll step if necessary
	End			

9.3 Advance Graphic Command

9.3.1 Set Fade Out / Fade In and Blinking (23h)

This command allow to set the fade mode and adjust the time interval for each fade step. Below figures show the example of Fade Out mode and Blinking mode.

Figure 9-14 : Example of Fade Out mode

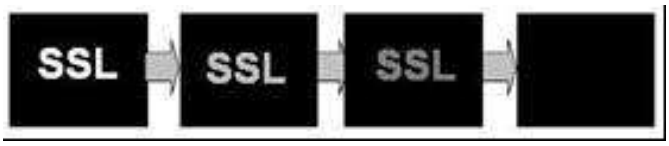


Figure 9-15 : Example of Fade In mode

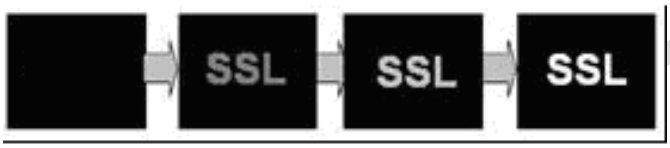
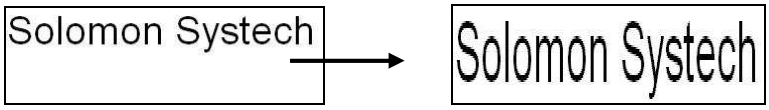


Figure 9-16 : Example of Blinking mode

9.3.2 Set Zoom In (D6h)

Under Zoom in mode, one row of display contents is expanded into two rows on the display. That is, contents of row0~31 fill the whole display panel of 39 rows. It should be notice that the panel must be in alternative COM pin configuration (command DAh A[4] =1) for zoom in function.

Figure 9-17 : Example of Zoom In



10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{BAT}		-0.3 to +5	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}, V_{DD} =1.65 V to 3.3V, T_A = 25°C

Table 11-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	-	15	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{BAT}	Charge Pump Regulator Supply Voltage	-	3	-	4.2	V
Charge Pump V_{CC}	Charge Pump Output Voltage	V_{BAT} = 3V~4.2V, Output loading = 8mA	7	7.5	-	V
		V_{BAT} = 3.8V~4.2V, Output loading = 12mA	8.5	9	-	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{DD,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
$I_{CC,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12, Internal I_{REF} , No loading, Display ON, All ON	Contrast = FFh	-	450	500	uA
I_{DD}	V_{DD} Supply Current V_{DD} =2.8V, V_{CC} = 12, Internal I_{REF} , No loading, Display ON, All ON,		-	77	85	uA
I_{SEG}	Segment Output Current, V_{DD} = 2.8V, V_{CC}=12V, I_{REF}=10uA Display ON.	Contrast=FFh	144	160	176	uA
		Contrast=AFh	-	110	-	
		Contrast=7Fh	-	80	-	
		Contrast=3Fh	-	40	-	
		Contrast=0Fh	-	10	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:127] = Segment current at contrast setting = FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

12 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=1.65 to3.3V
T_A = 25°C

Table 12-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.8V	382	425	468	kHz
FFRM	Frame Frequency for 39 MUX Mode	128x39 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx39) (2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

(2) D: divide ratio (default value = 2)
K: number of display clocks per row period (default value = 54)

Table 12-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 12-1 : 6800-series MCU parallel interface characteristics

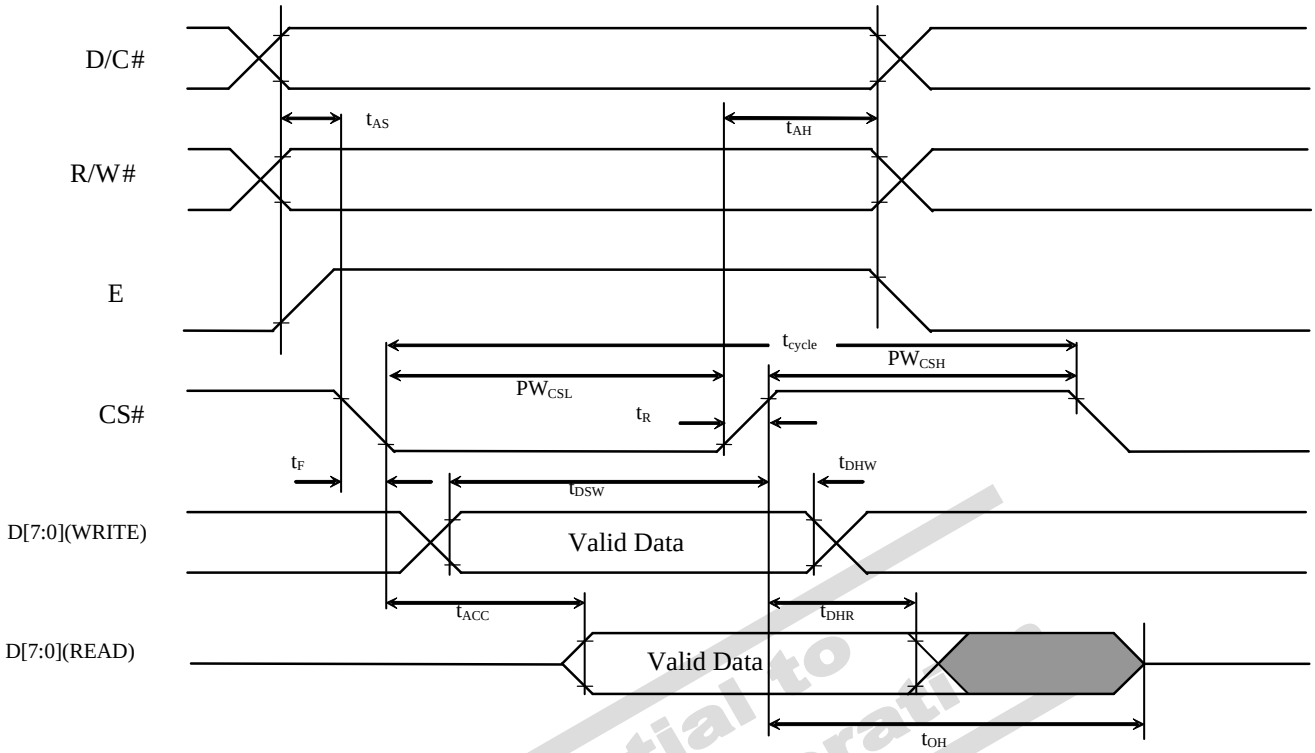


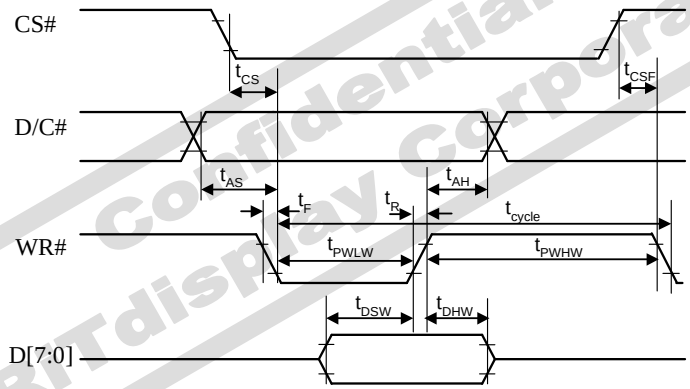
Table 12-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V ~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 12-2 : 8080-series parallel interface characteristics

Write cycle



Read Cycle

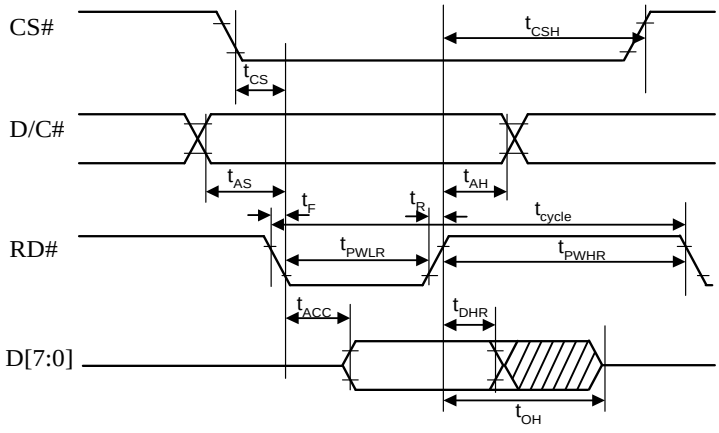


Table 12-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	40	-	-	ns
t_{CLKH}	Clock High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 12-3 : Serial interface characteristics (4-wire SPI)

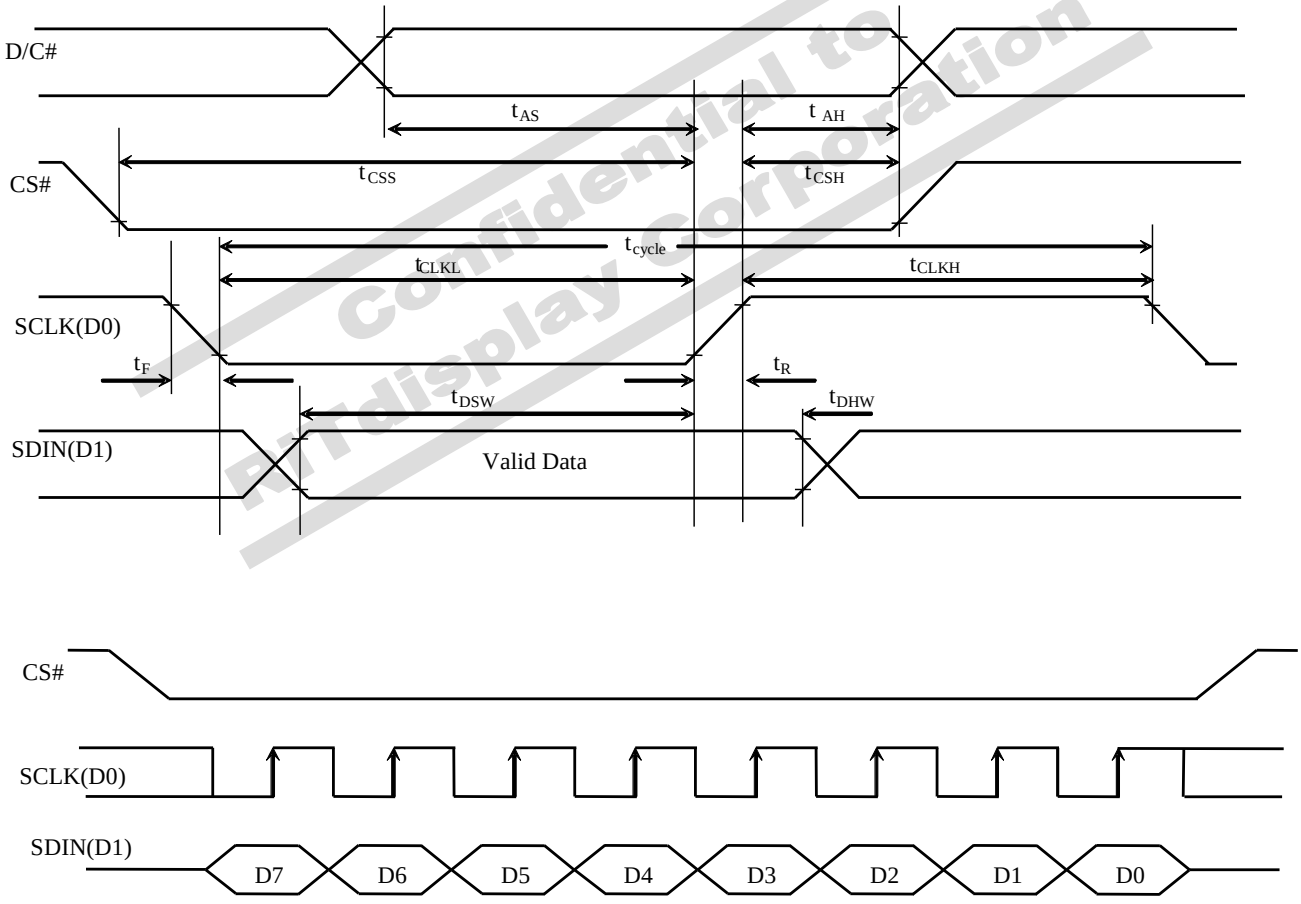
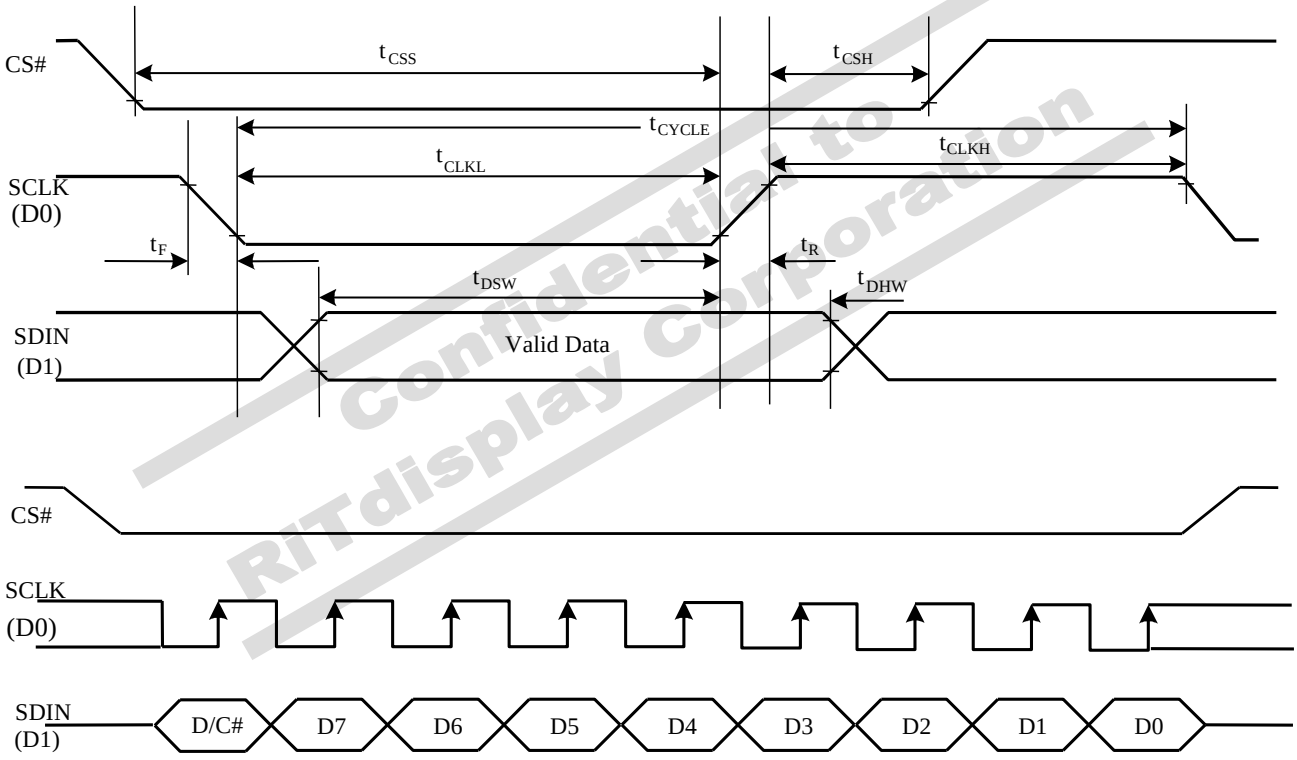


Table 12-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	40	-	-	ns
t_{CLKH}	Clock High Time	40	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 12-4 : Serial interface characteristics (3-wire SPI)



Conditions:

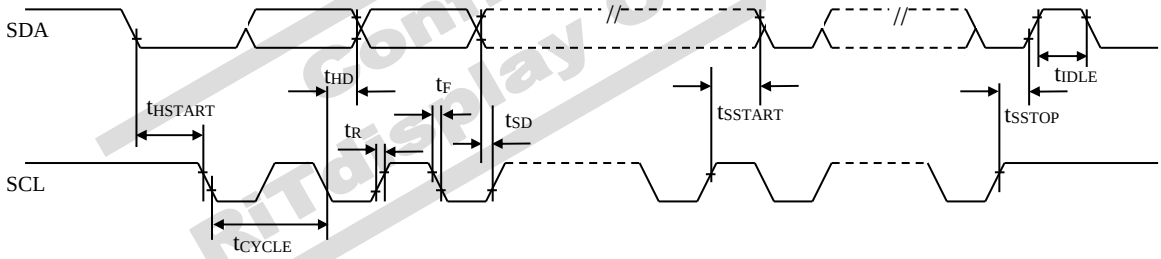
V_{DD} - V_{SS} = 1.65V ~ 3.3V

T_A = 25°C

Table 12-6 : I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

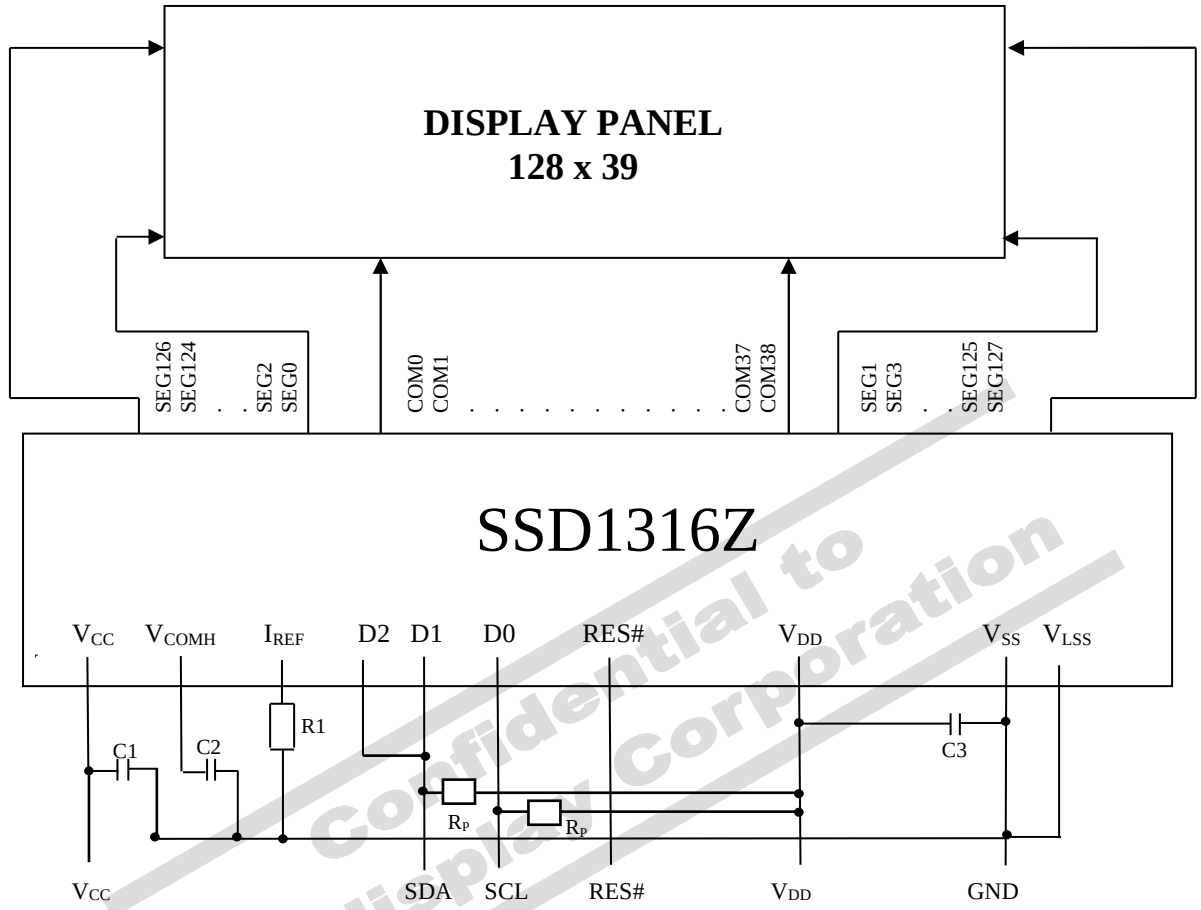
Figure 12-5 : I²C interface Timing characteristics



13 APPLICATION EXAMPLES

Figure 13-1 : Application Example of SSD1316Z with External V_{CC} and I^2C Interface

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DD}=2.8V, V_{CC} =12V, I_{REF}=10uA)



Pin connected to MCU interface: D[2:0], RES#
Pin internally connected to V_{SS}: D[7:3], BS0, BS2, E, R/W#, CS#, CL, BGGND
Pin internally connected to V_{DD}: BS1, CLS
VBREF, FR should be left open.
D/C# acts as SA0 for slave address selection (3)

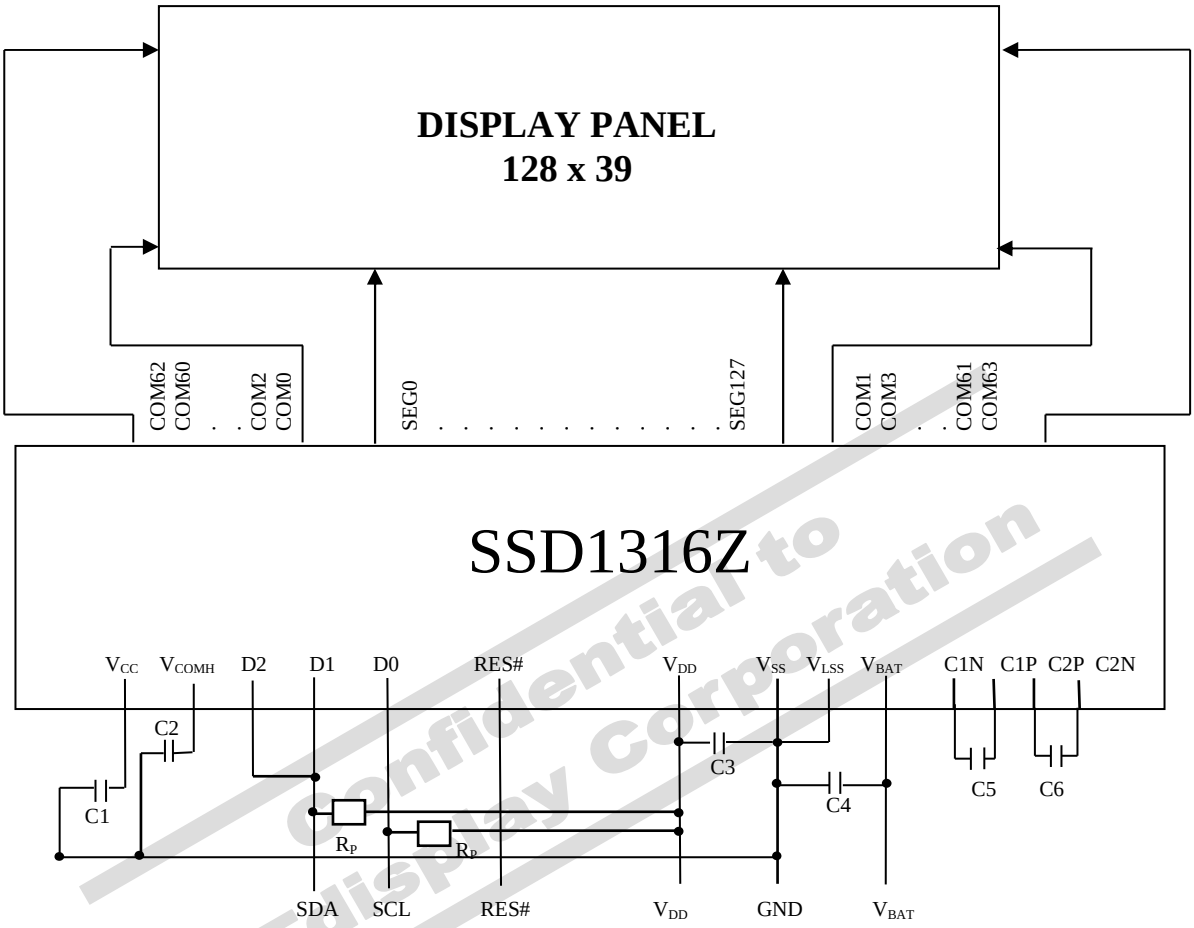
C1, C2: 2.2uF (1)
C3: 1.0uF (1) place close to IC VDD and VSS pins on PCB
R_P : Pull up resistor

Voltage at I_{REF} = V_{CC} – 5V. For V_{CC} = 12V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
≈ (12-5)V / 10uA
= 700KΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face down.
(3) Refer to Section 7.1.5 for details.

Figure 13-2 : Application Example of SSD1316Z with Internal Charge Pump, Internal I_{REF} and I^2C interface

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DD}=2.8V, V_{BAT} =3.8V, Internal I_{REF})



Pin connected to MCU interface: RES#, D[2:0]
Pin internally connected to V_{SS}: BS0, BS2, CL, D[7:3], E, R/W#, CS#, D/C#, BGGND
Pin internally connected to V_{DD}: BS1, CLS
I_{REF}, V_{BREF}, FR should be left open.

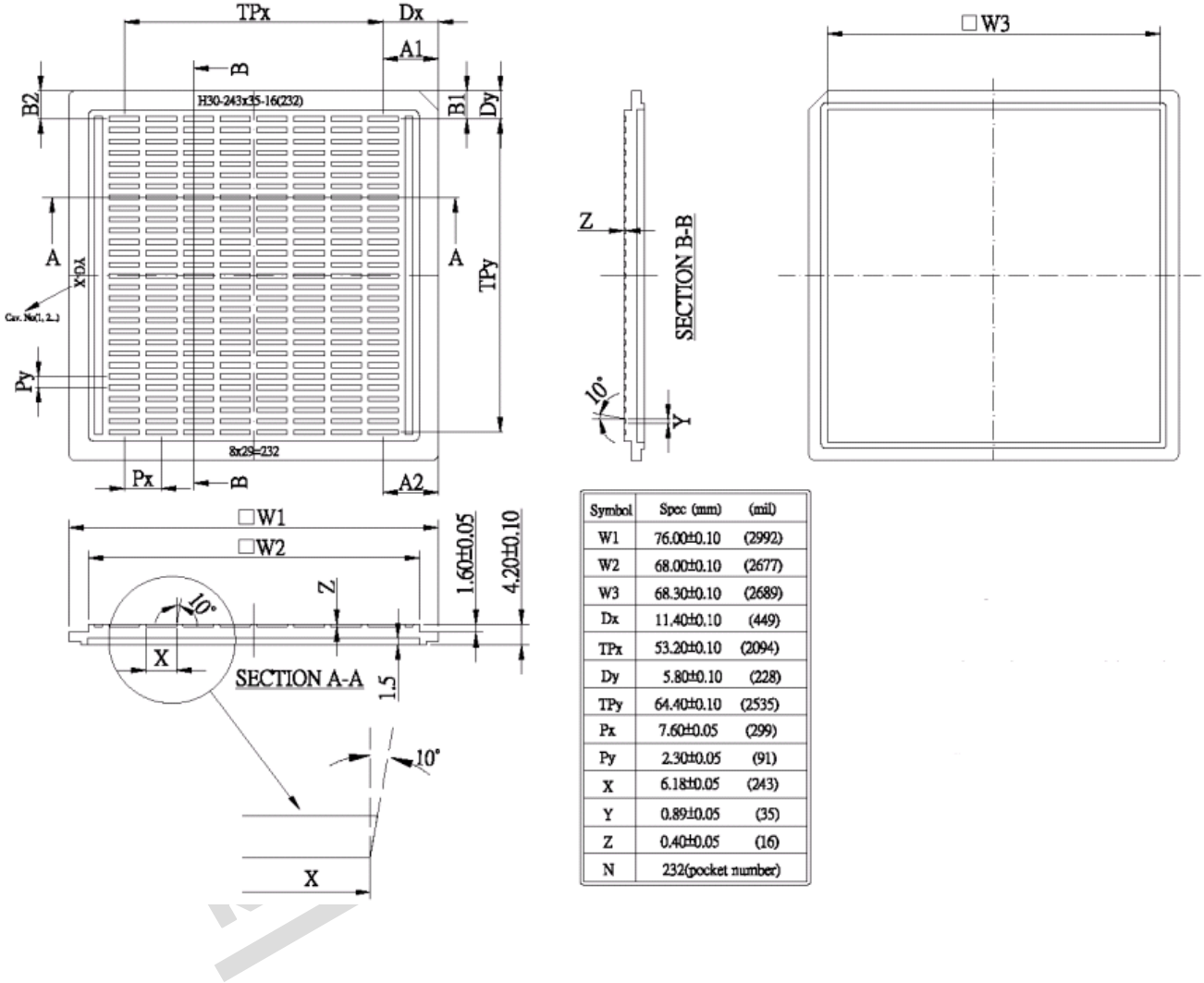
C1, C2: 2.2uF (1)
C3, C4 : 1.0uF (1)
C5, C6: 1.0uF/10V (1)
R_P : Pull up resistor

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

14 PACKAGE INFORMATION

14.1 DIE TRAY DIMENSIONS

Figure 14-1 : SSD1316Z die tray information



Symbol	Spec (mm)	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
Dx	11.40±0.10	(449)
TPx	53.20±0.10	(2094)
Dy	5.80±0.10	(228)
TPy	64.40±0.10	(2535)
Px	7.60±0.05	(299)
Py	2.30±0.05	(91)
X	6.18±0.05	(243)
Y	0.89±0.05	(35)
Z	0.40±0.05	(16)
N	232(pocket number)	

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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